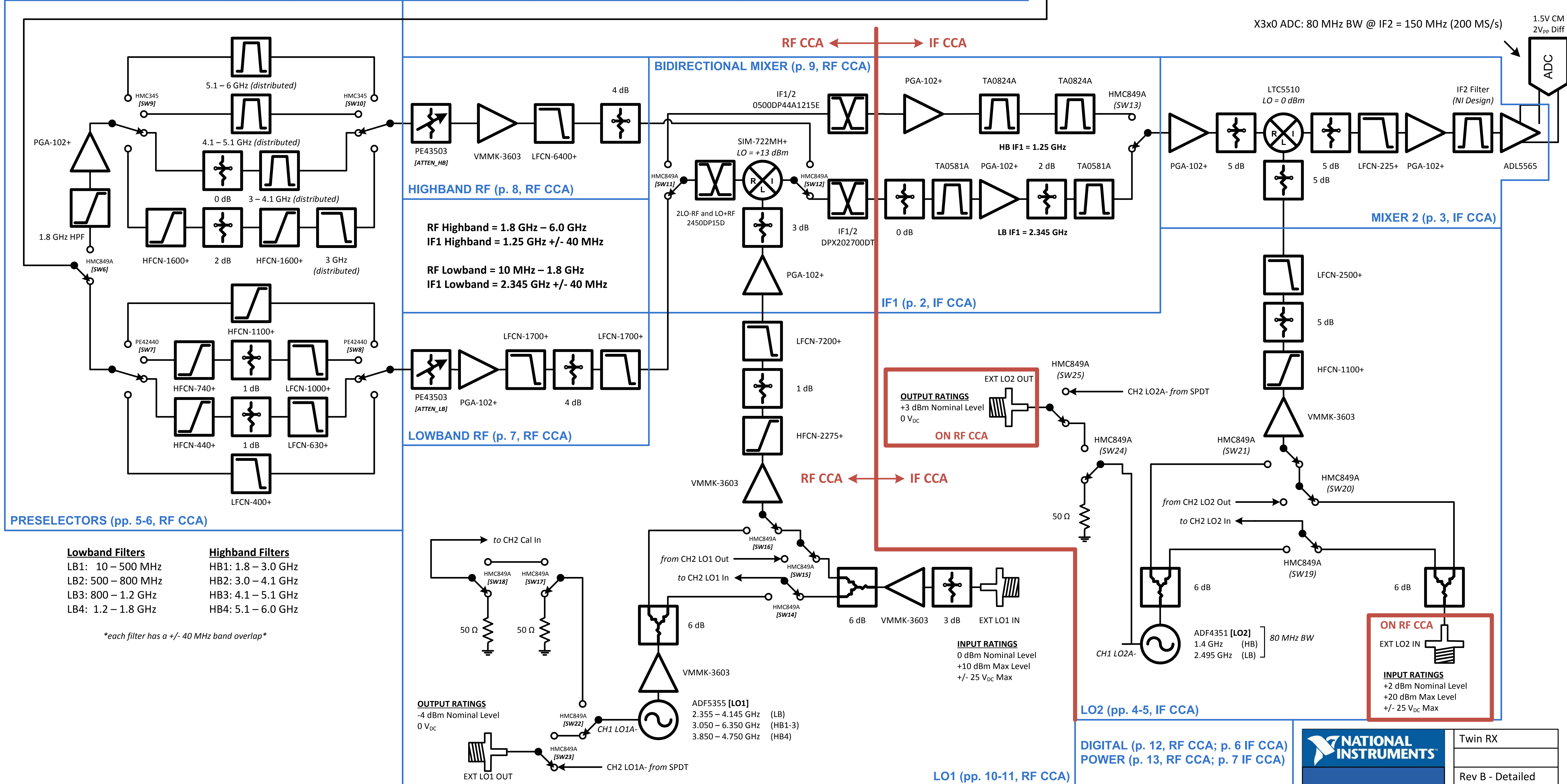


This block diagram represents one channel of a two-channel 10 MHz to 6 GHz superheterodyne daughterboard for the X3x0 (80 MHz BW) platform.

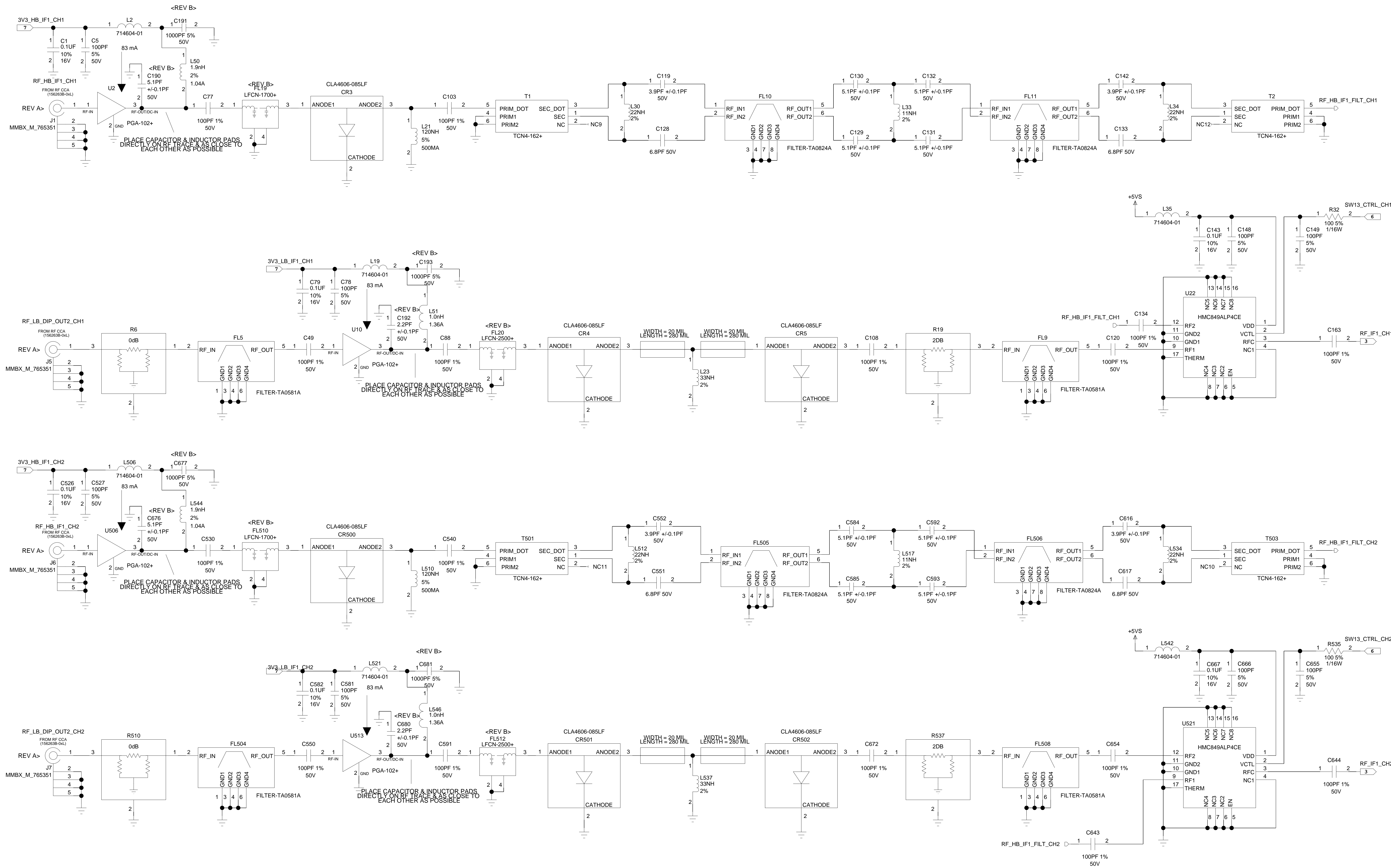
There are two LOs per channel, utilizing the ADF5355 and ADF4351 synthesizers, synchronized via FPGA I/O lines. Switchable LO input/output ports exist between channels.



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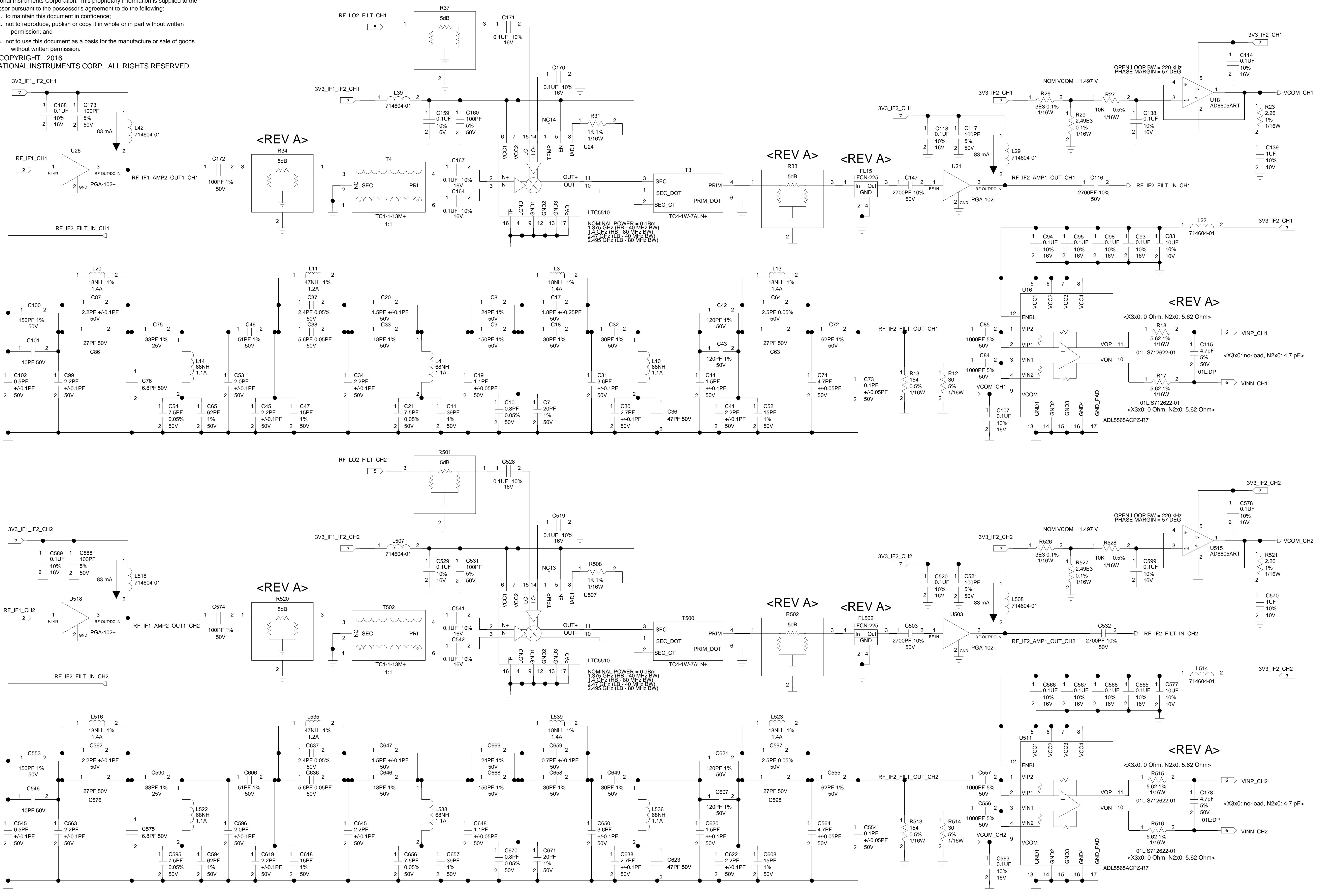


2-IF1			
TWINRX USRP IF BD			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	158672C-01	2
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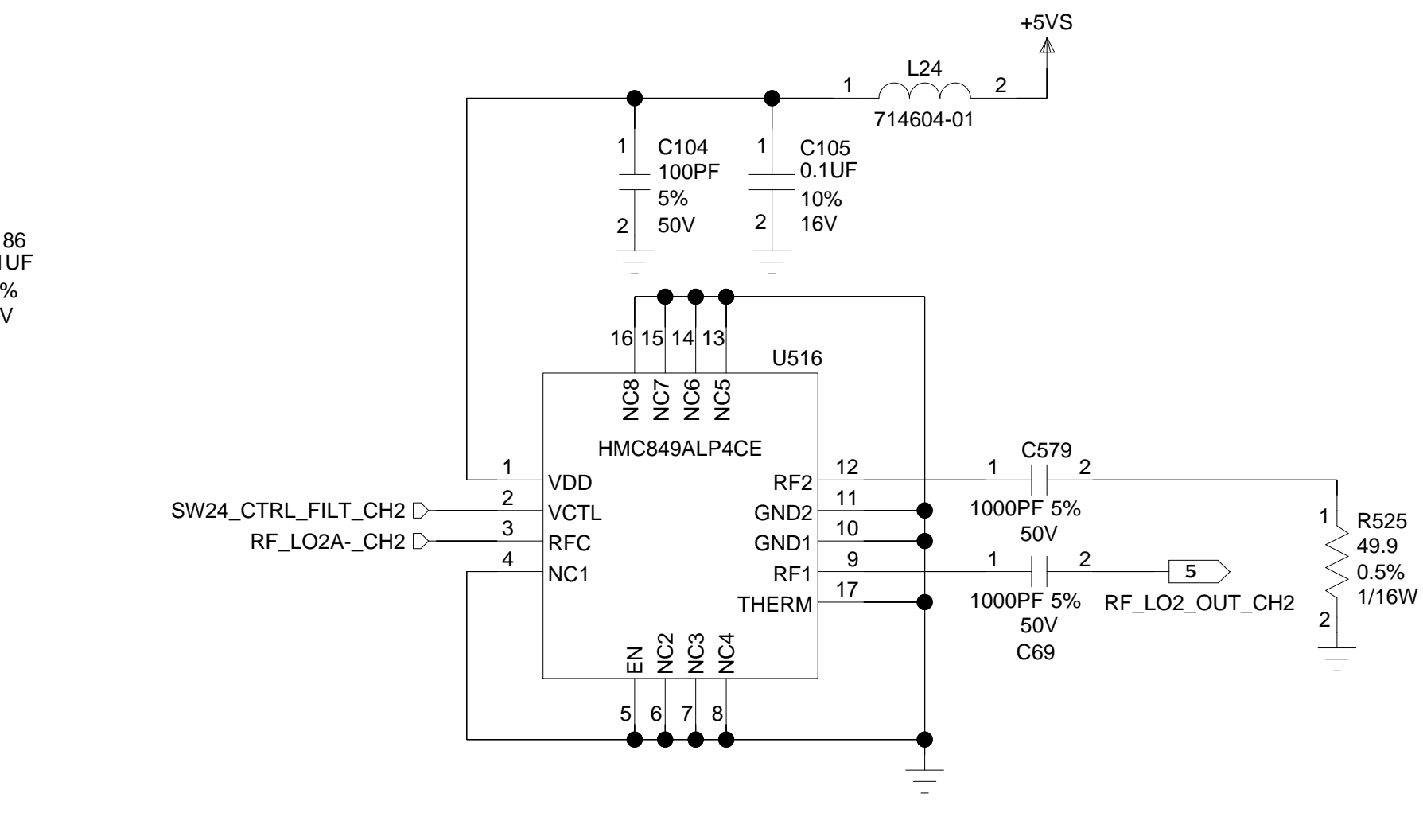
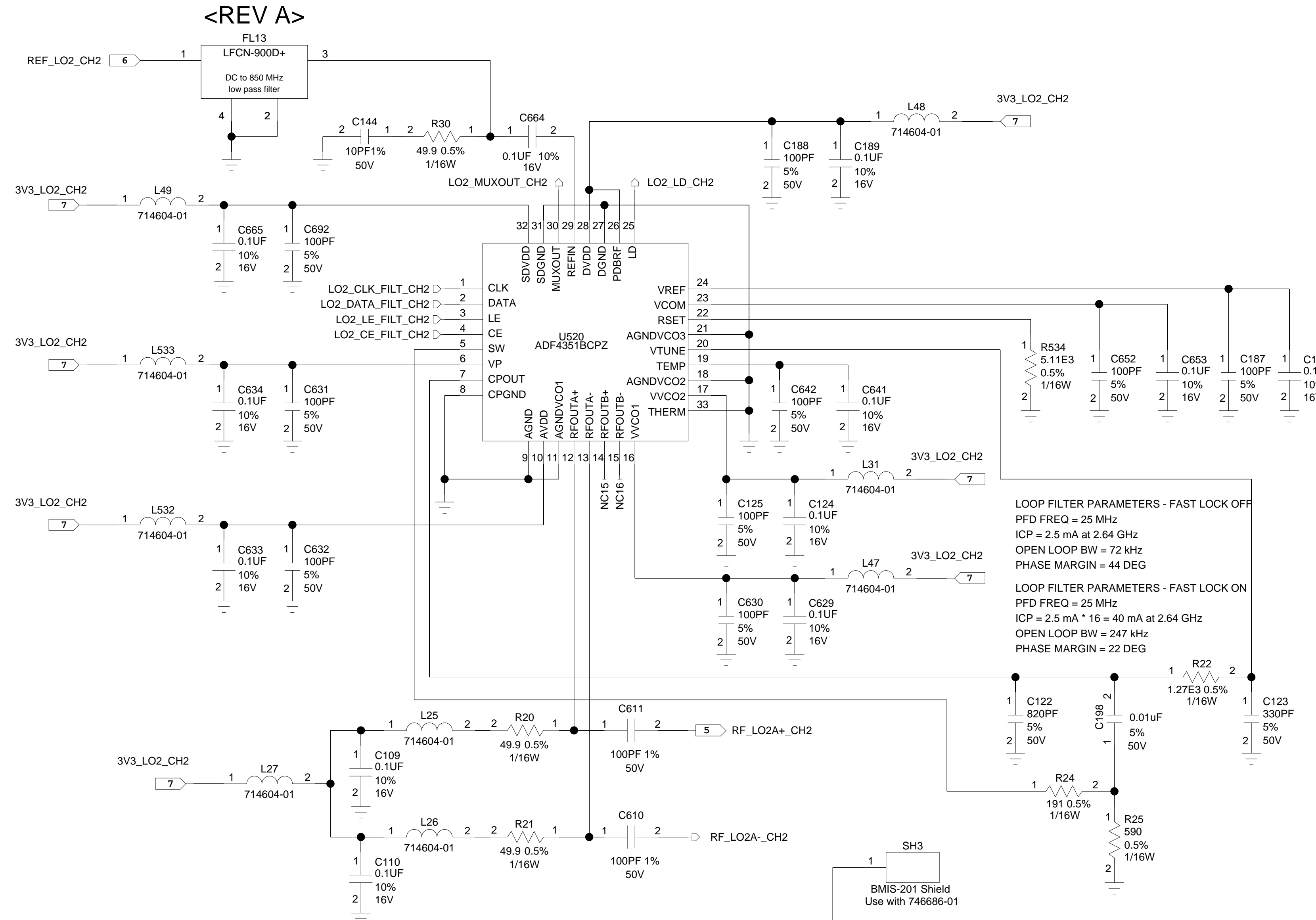
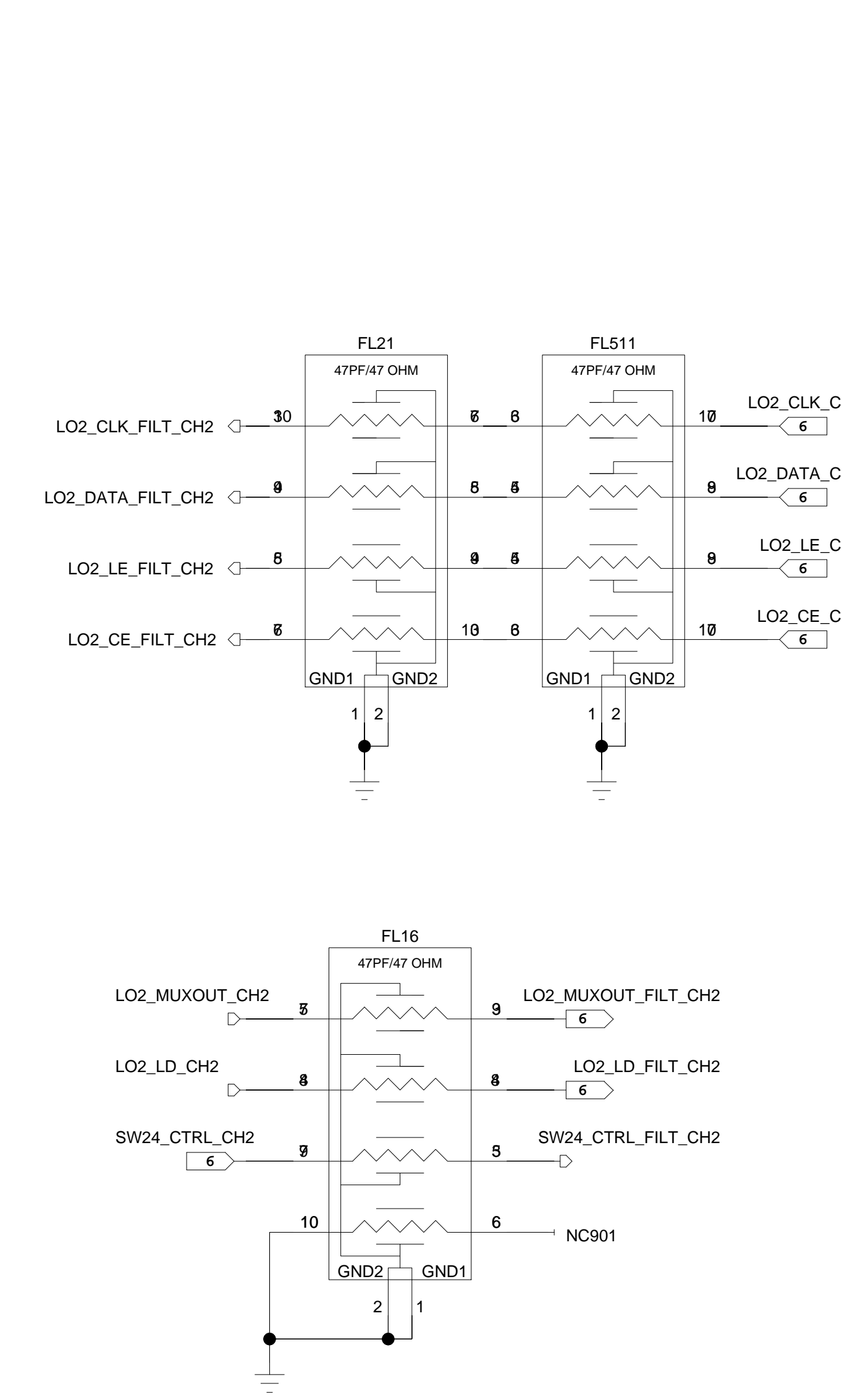
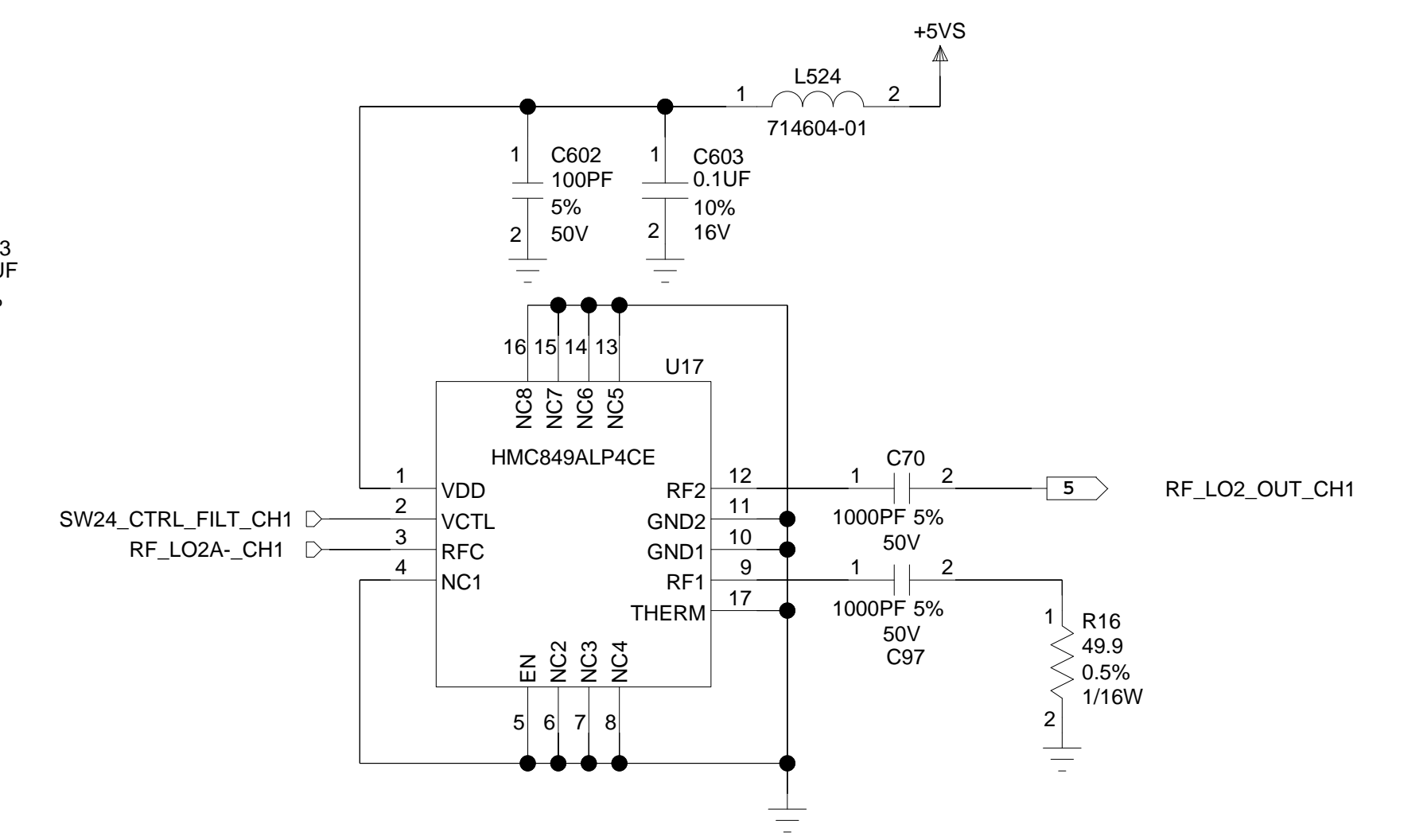
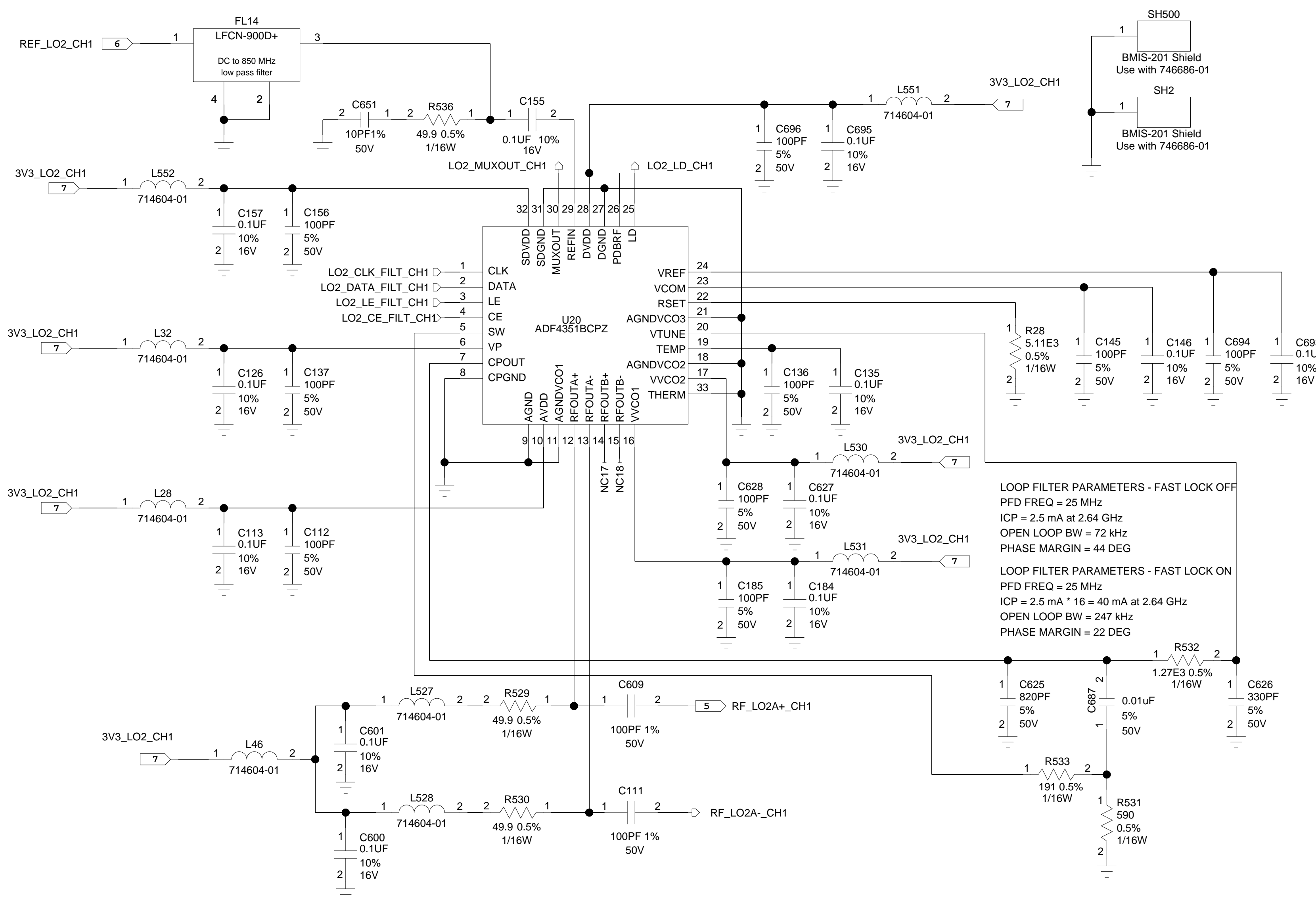
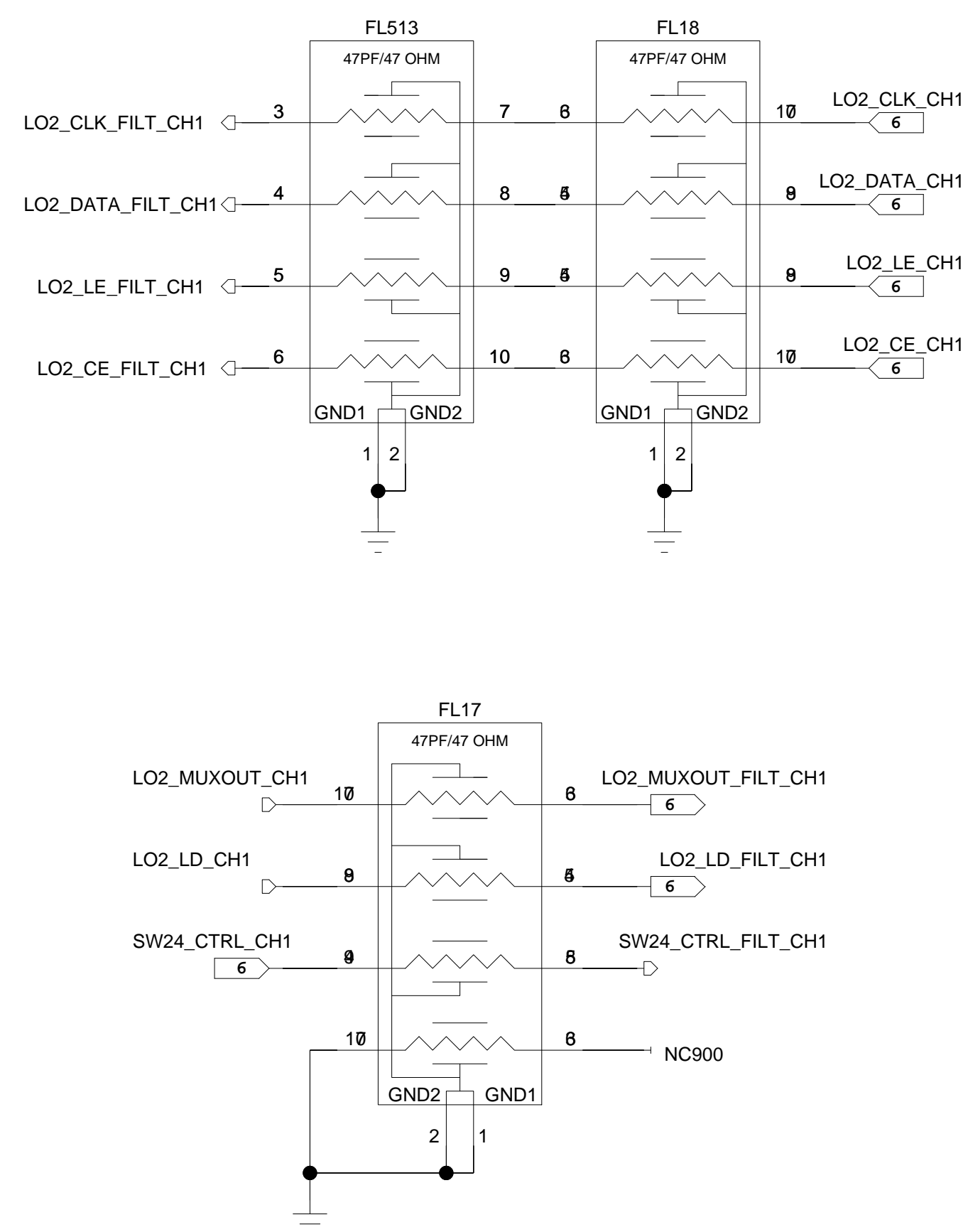


3-Mixer 2			
TWINRX USRP IF BD			
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C	7U296	158672C-01	2
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4-LO2 Synthesizer			
TWINRX USRP IF BD			
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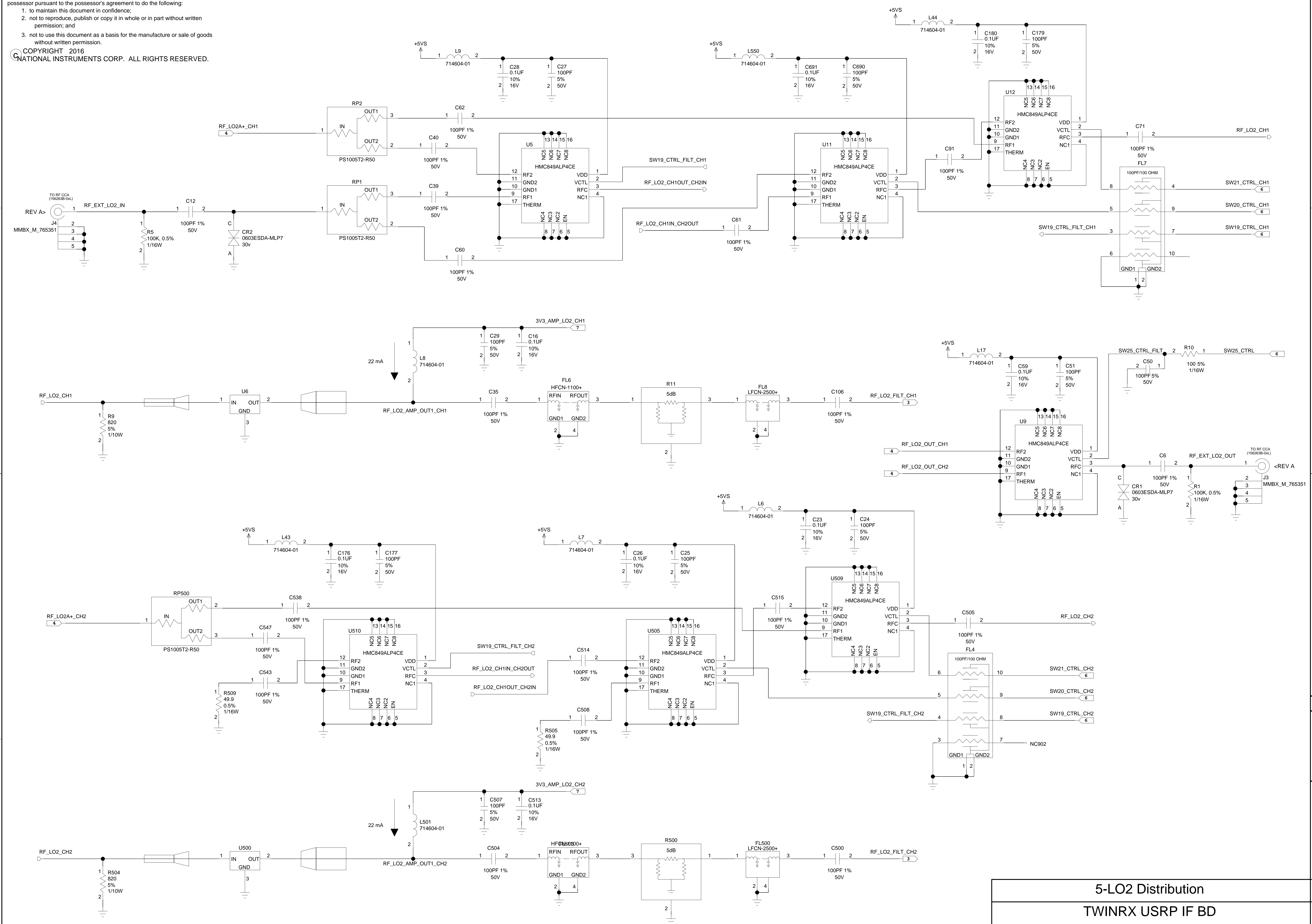
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D

C

B

A



5-LO2 Distribution			
TWINRX USRP IF BD			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	158672C-01	2
SCALE: NONE		SHEET 5 OF 7	

4

3

2

1

D

C

B

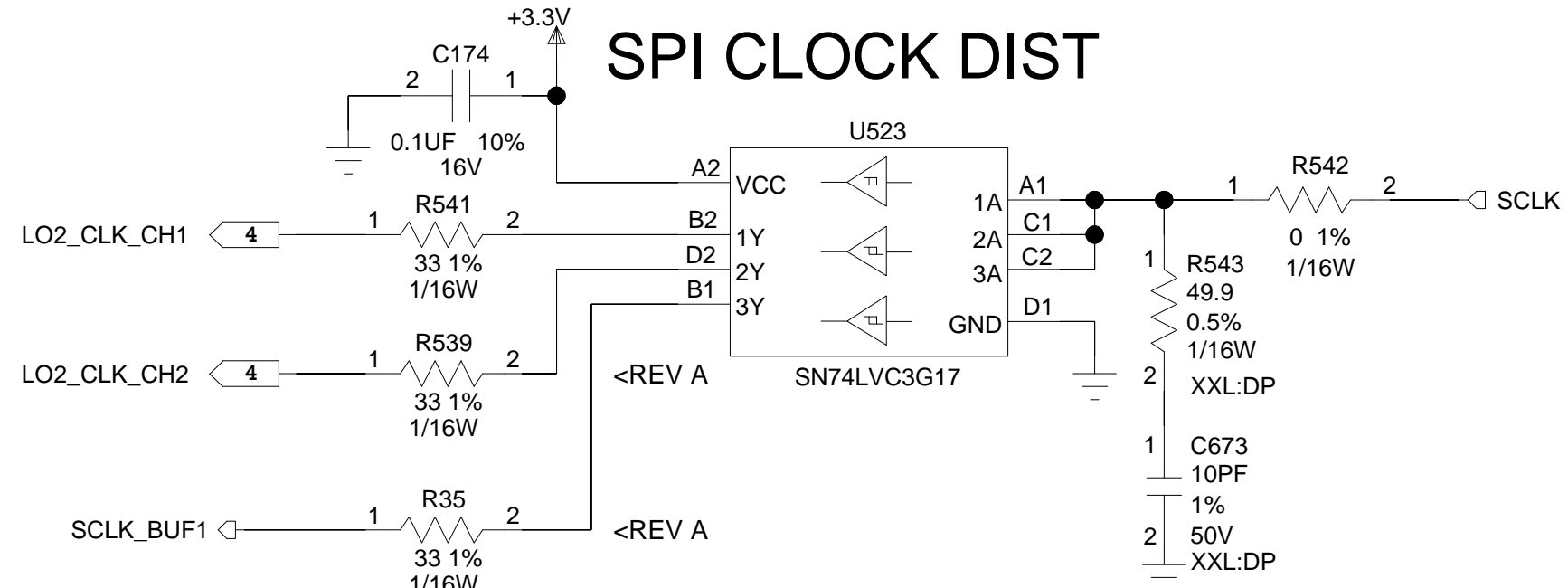
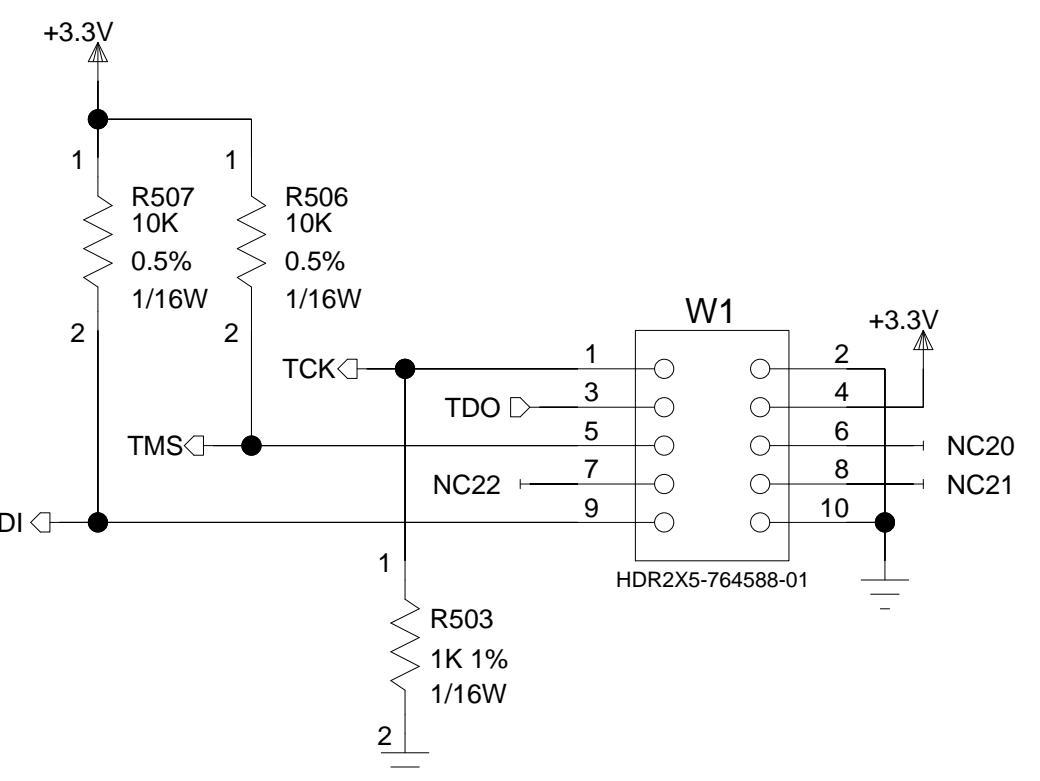
A

R

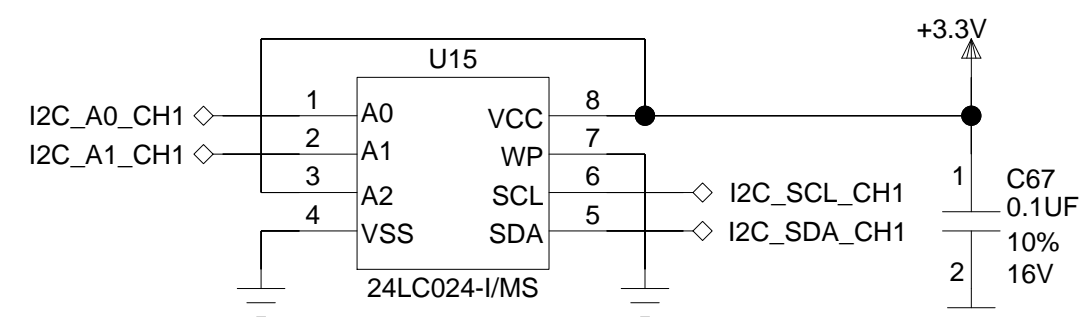
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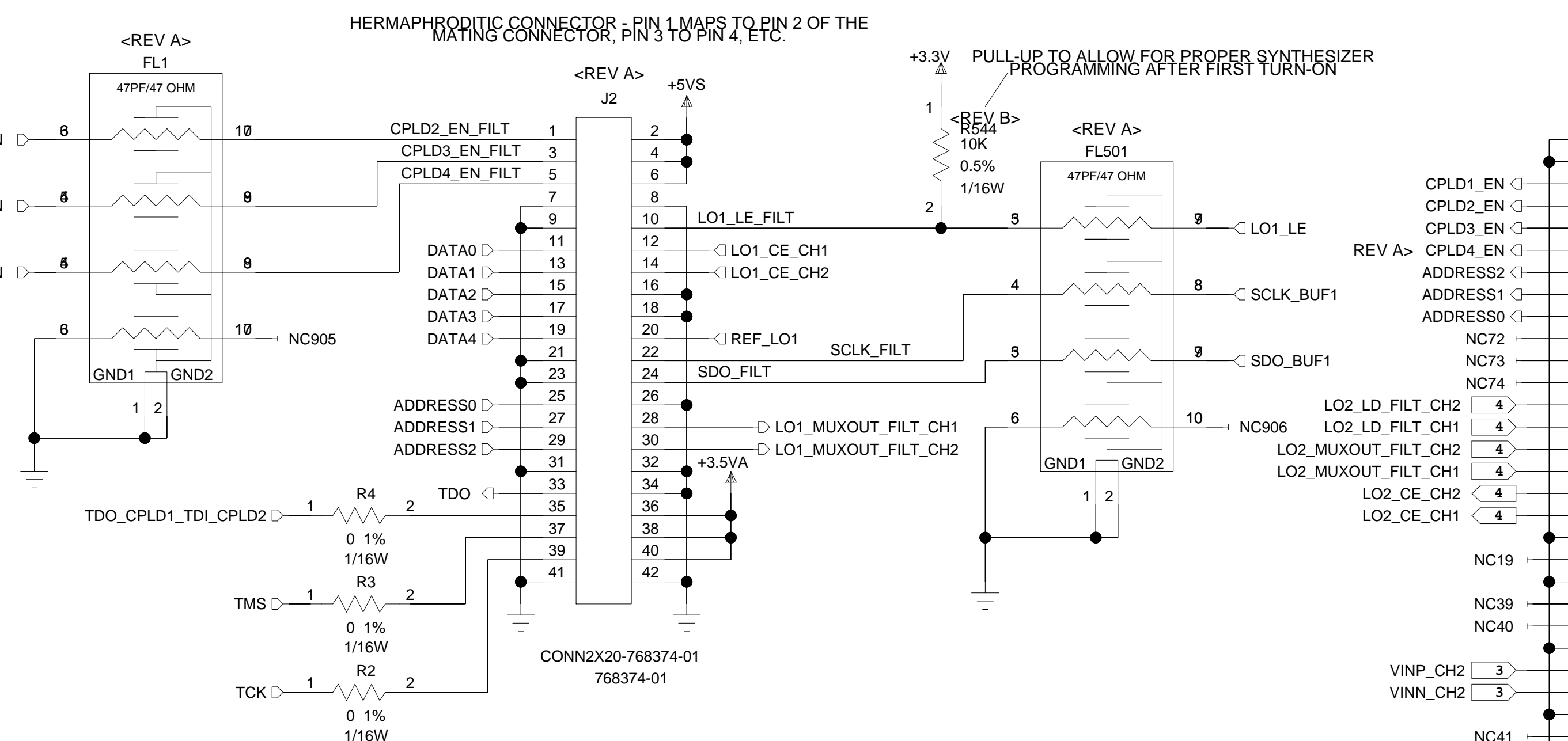
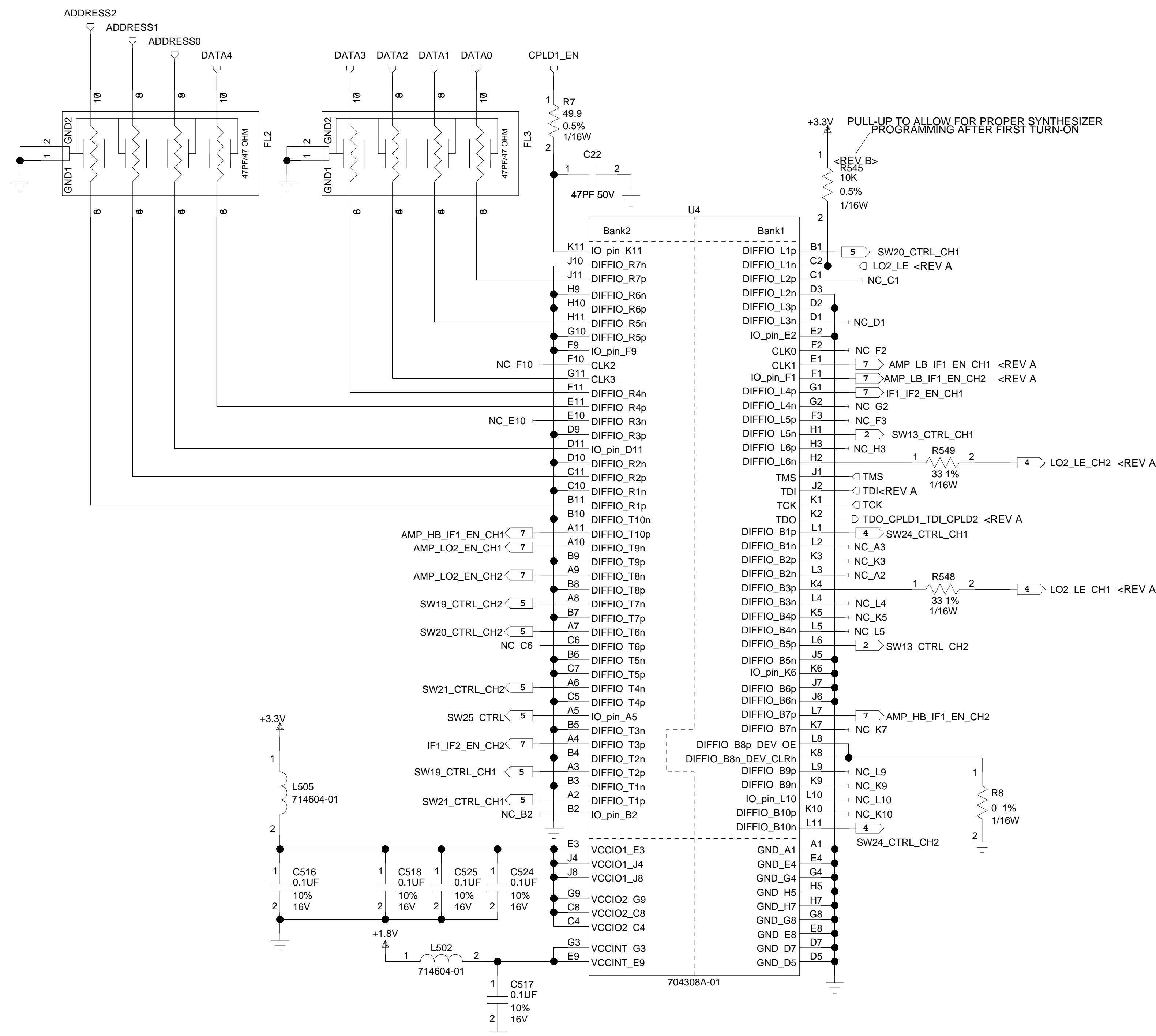
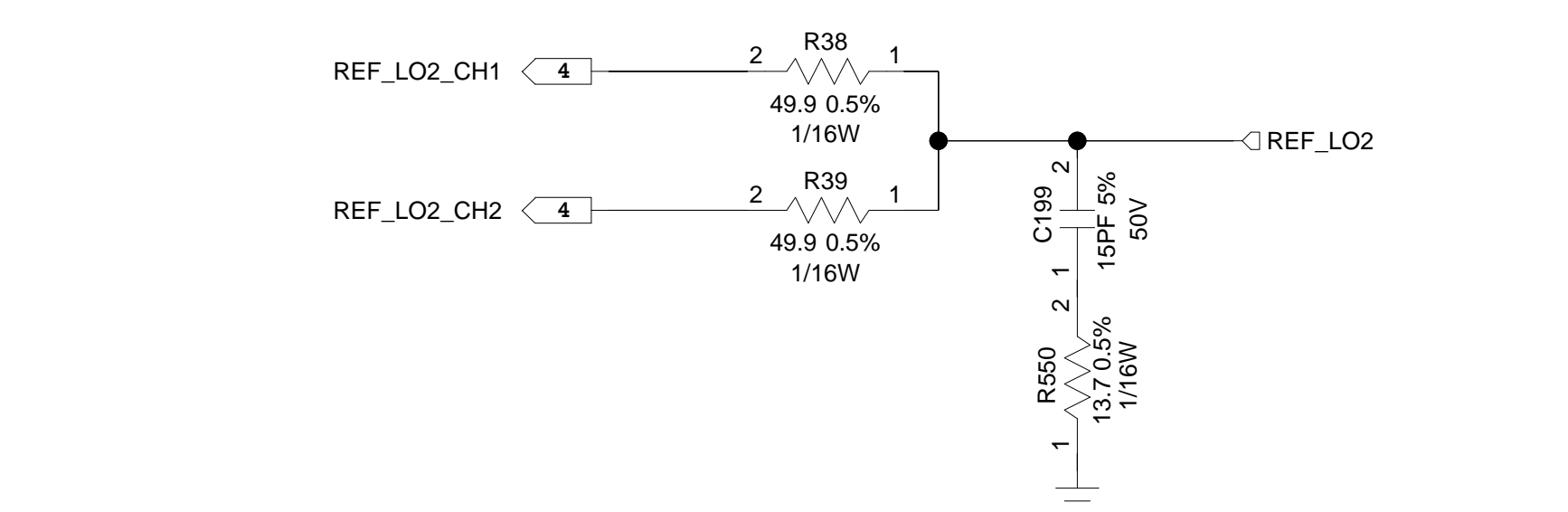
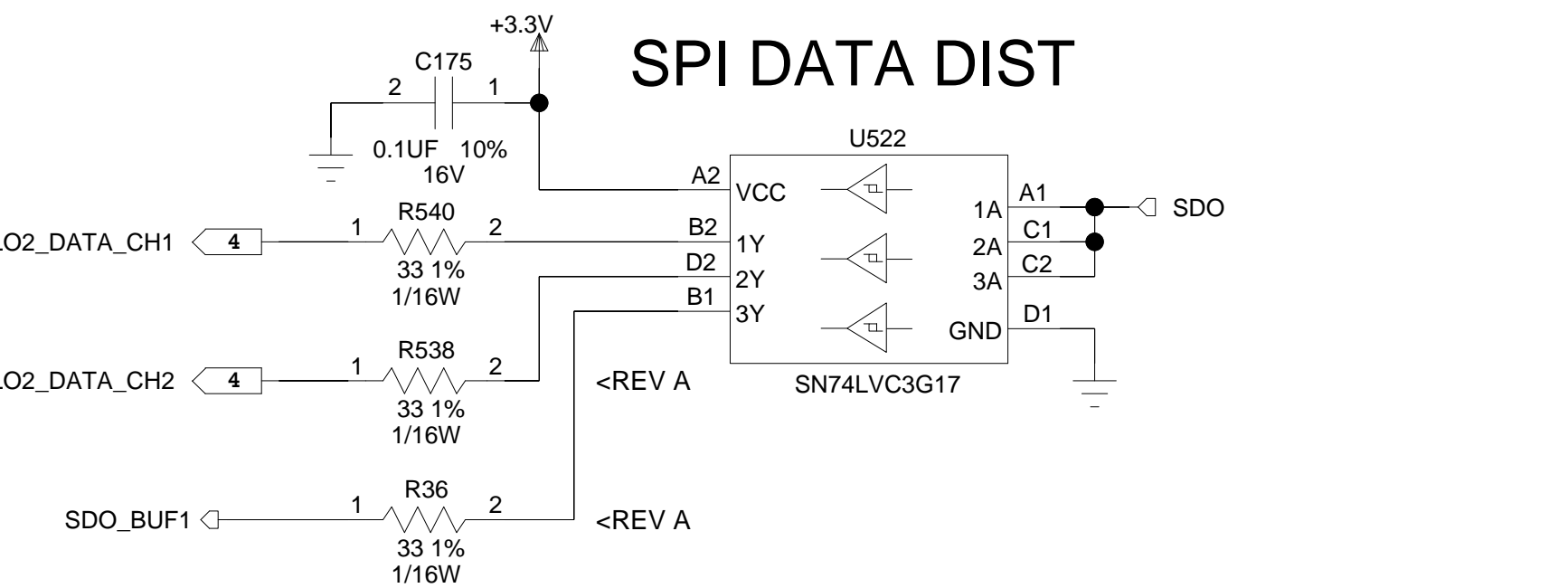
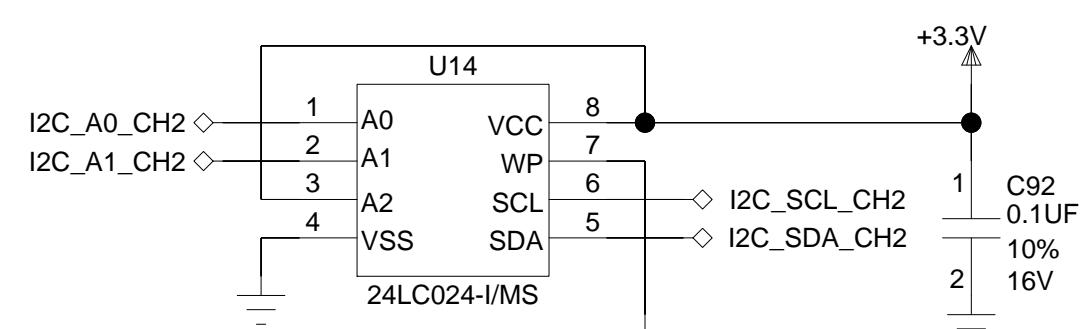
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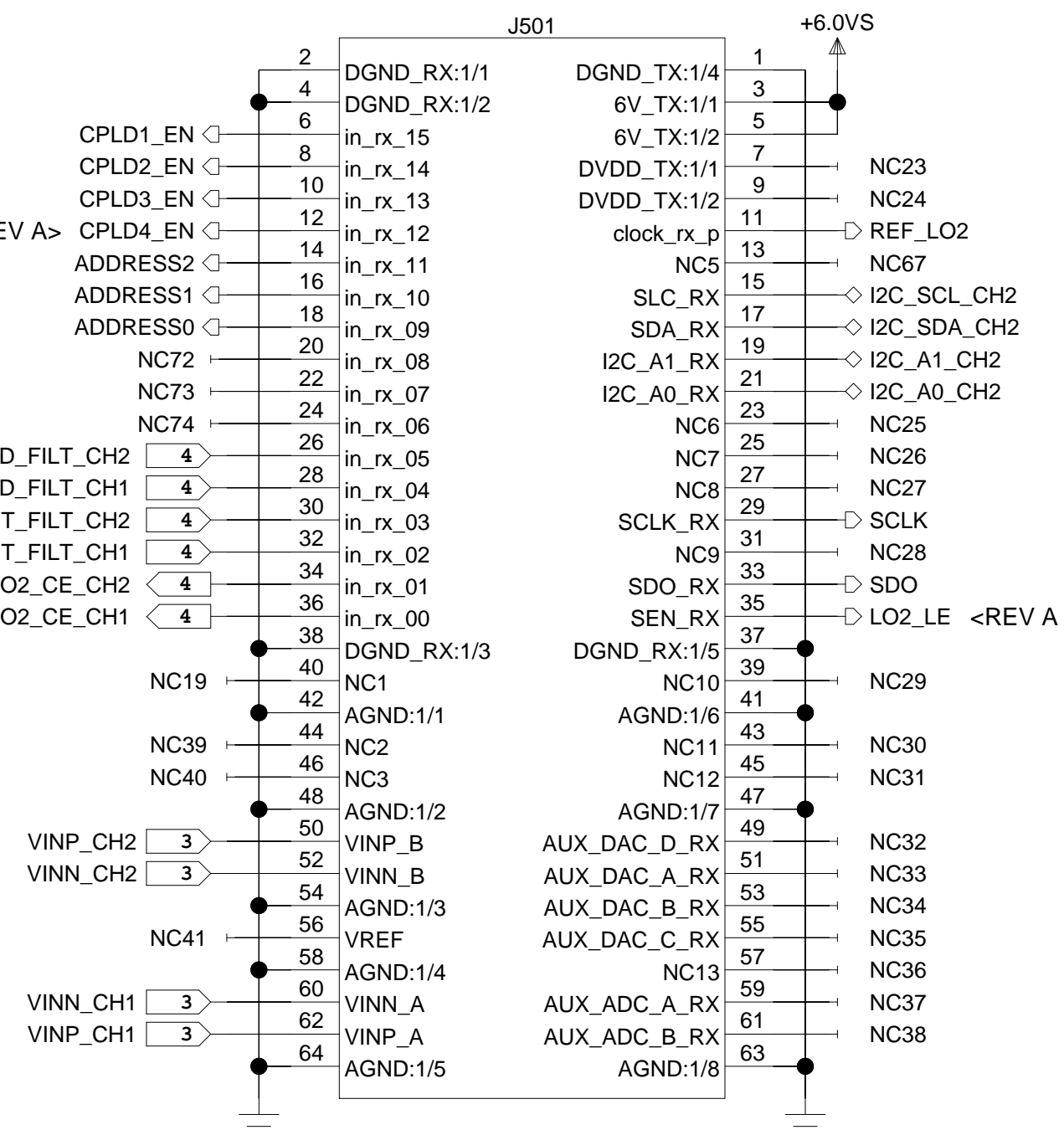
CH1 EEPROM



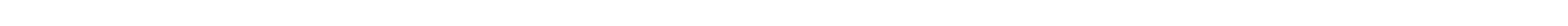
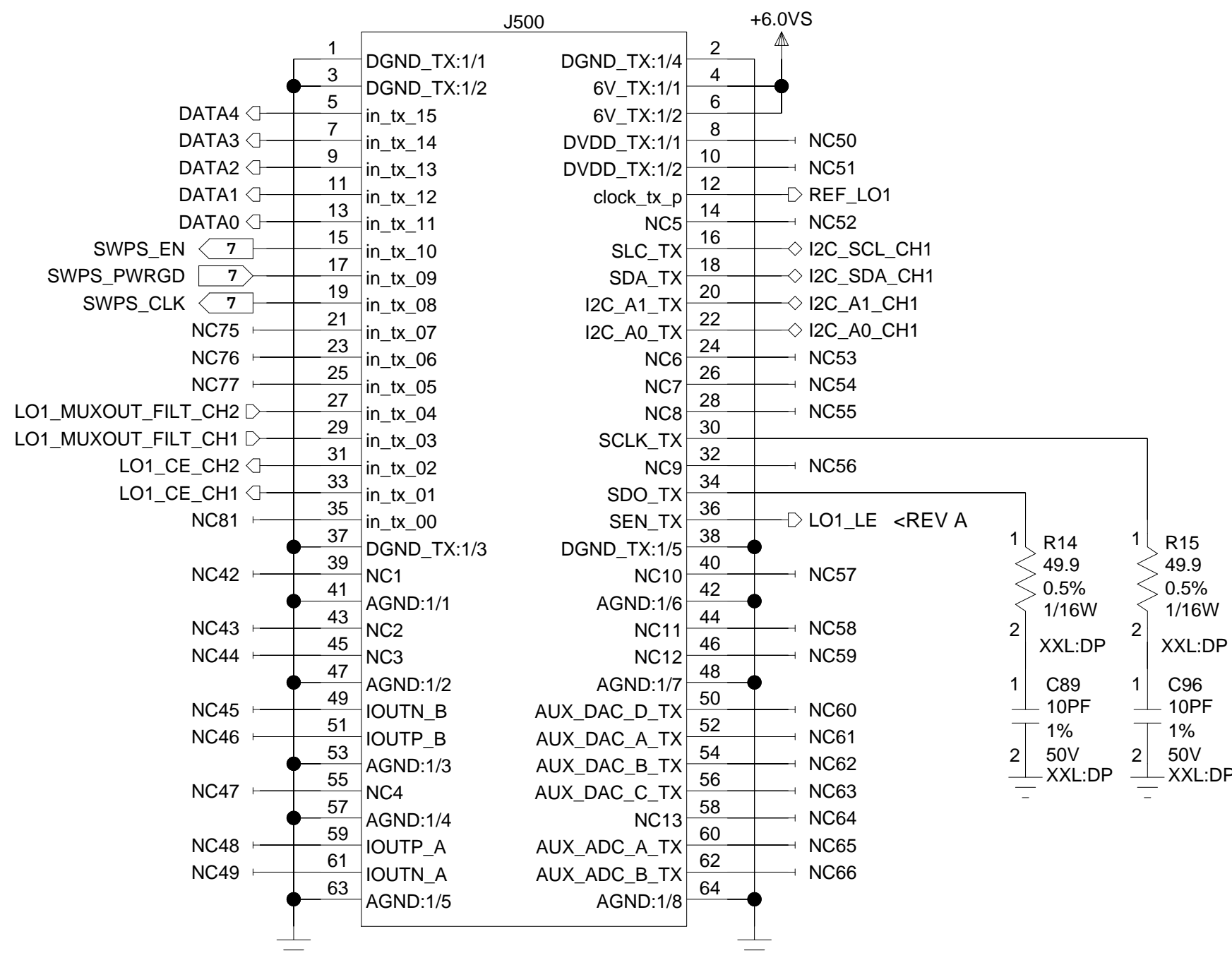
CH2 EEPROM



LO2 CONN



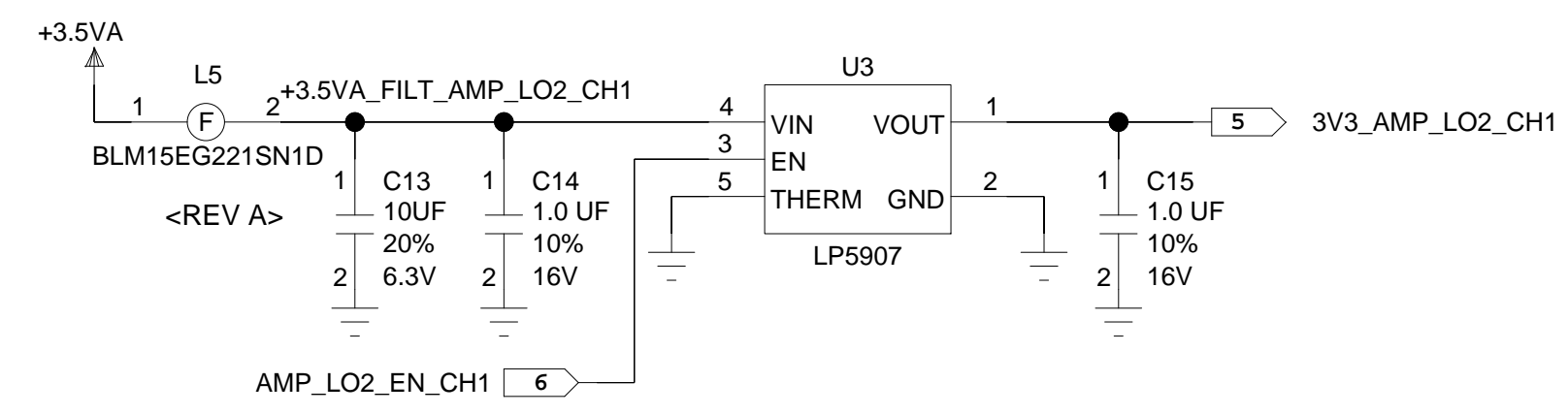
LO1 CONN



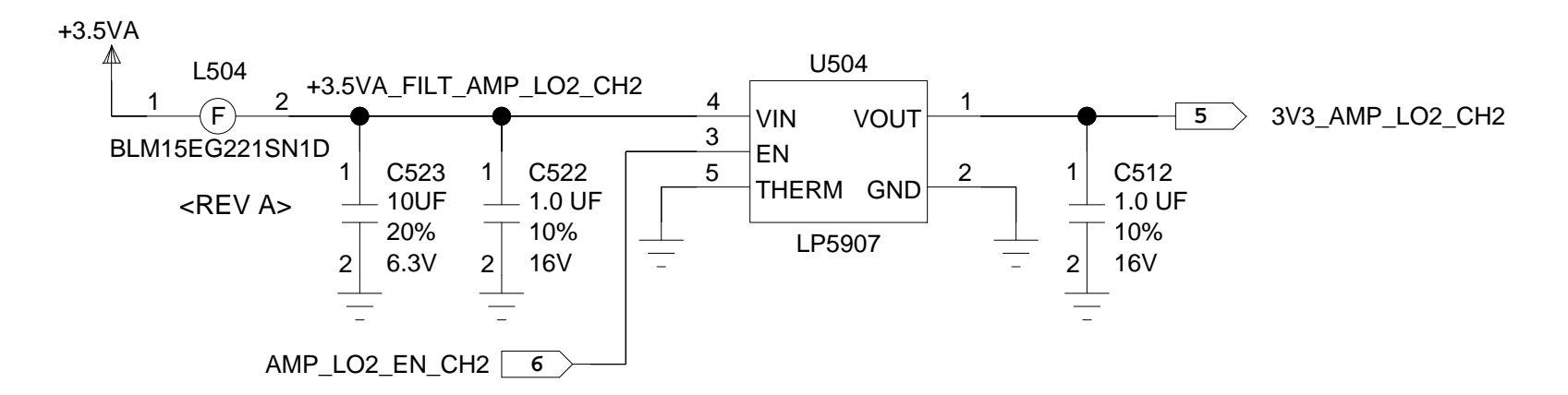
6-Digital-MB Interface			
TWINRX USRP IF BD			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
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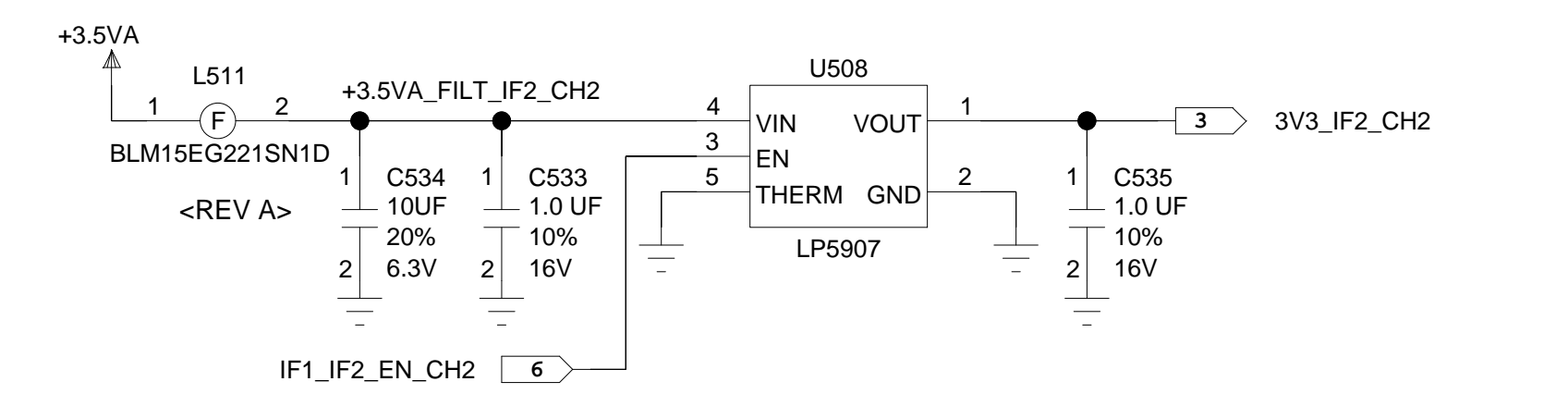
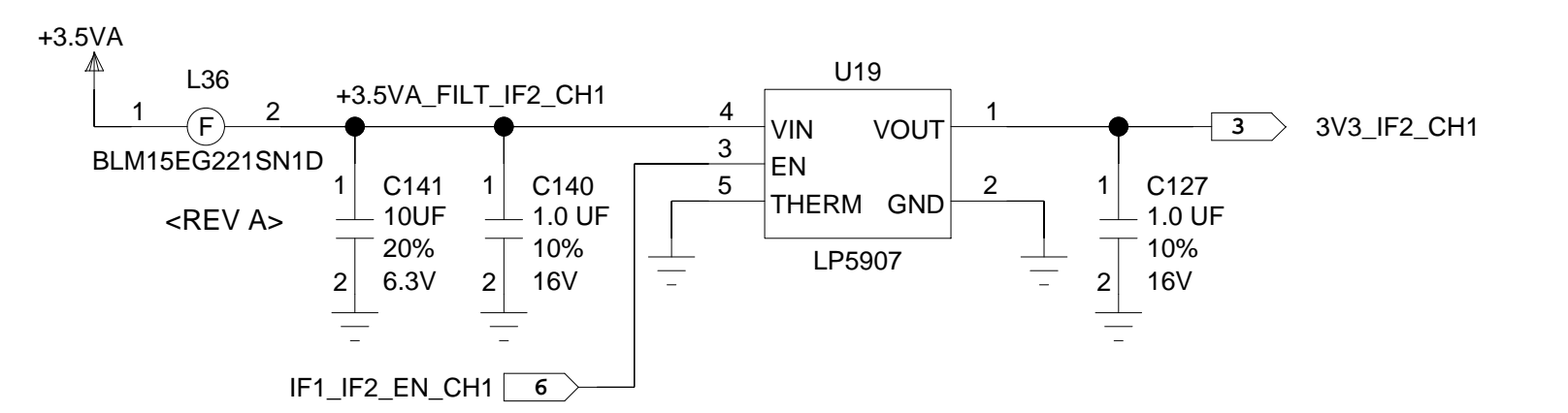
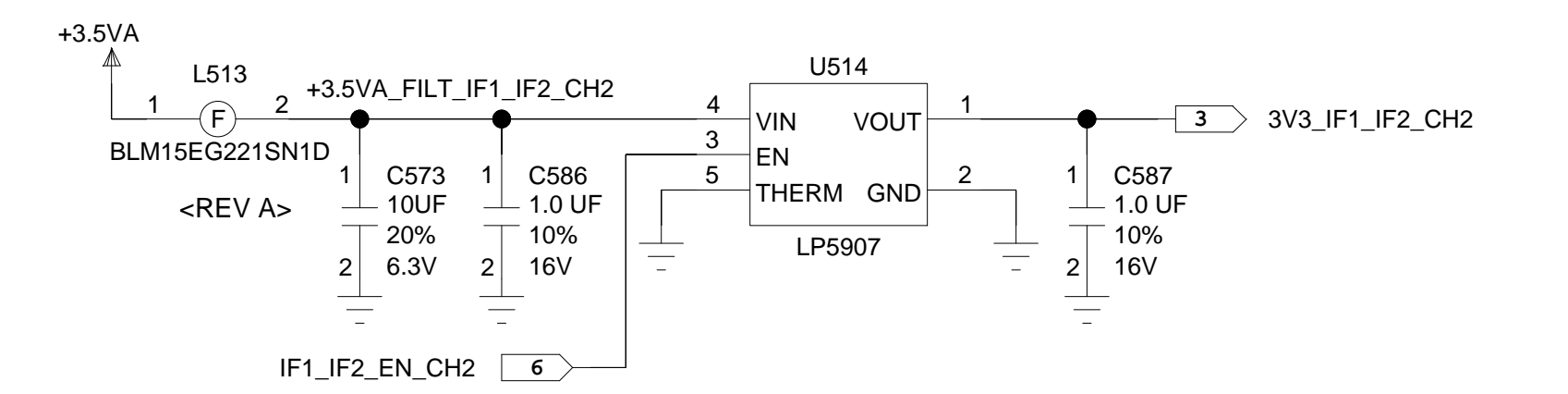
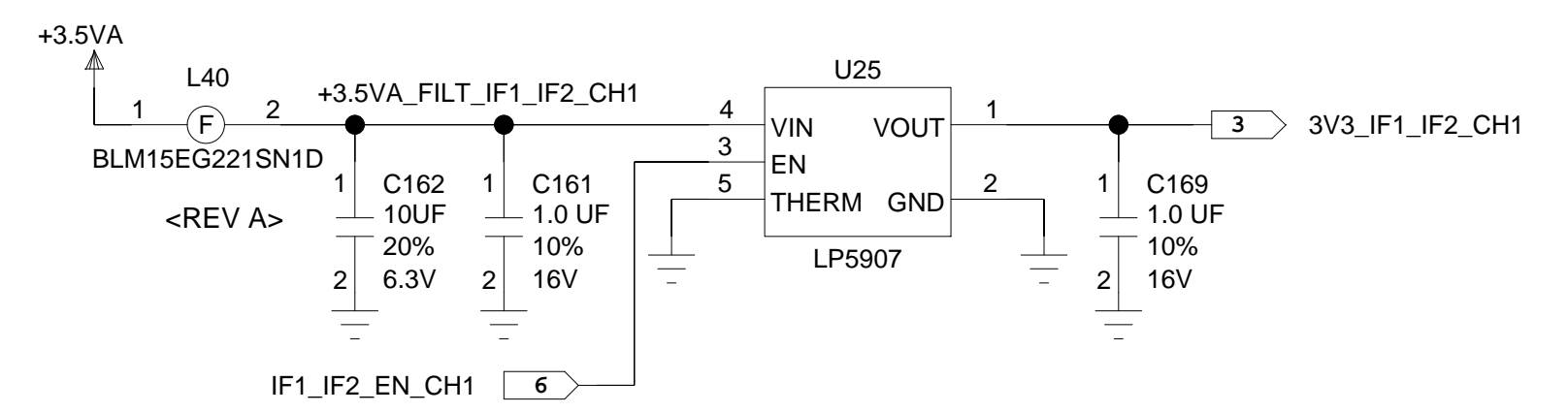
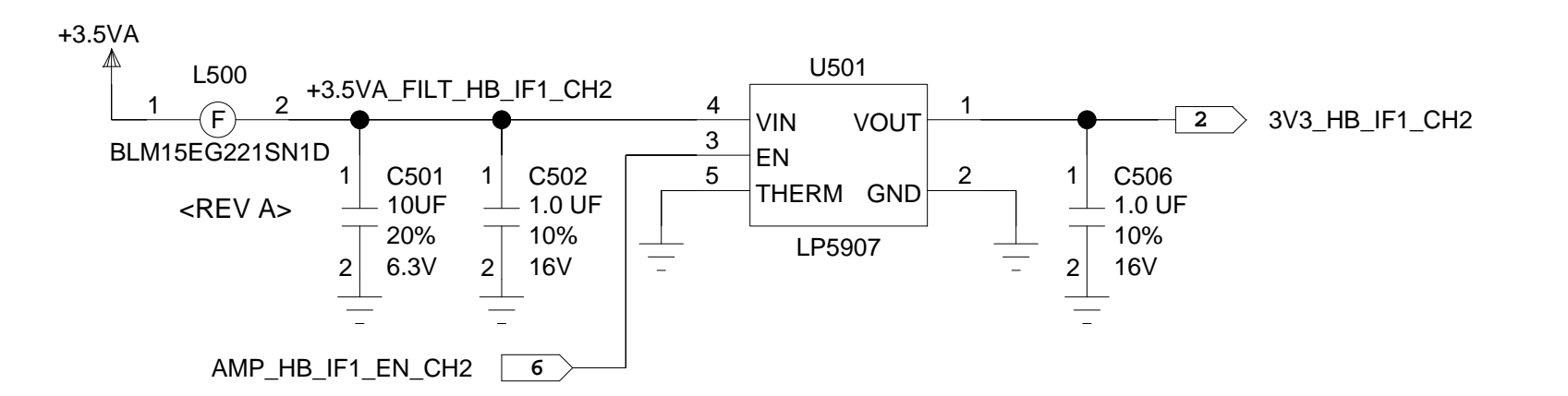
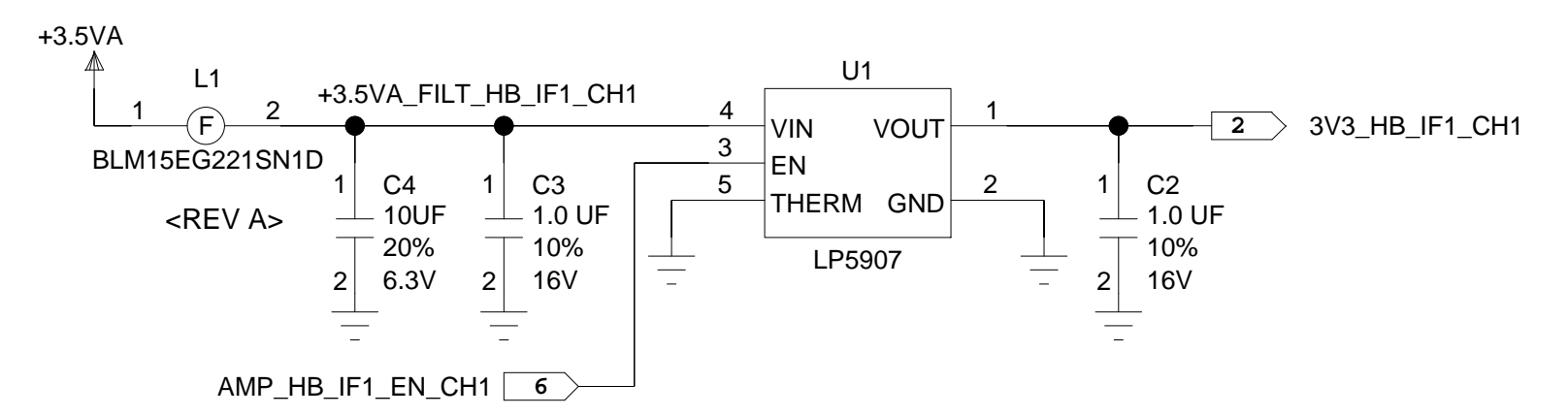
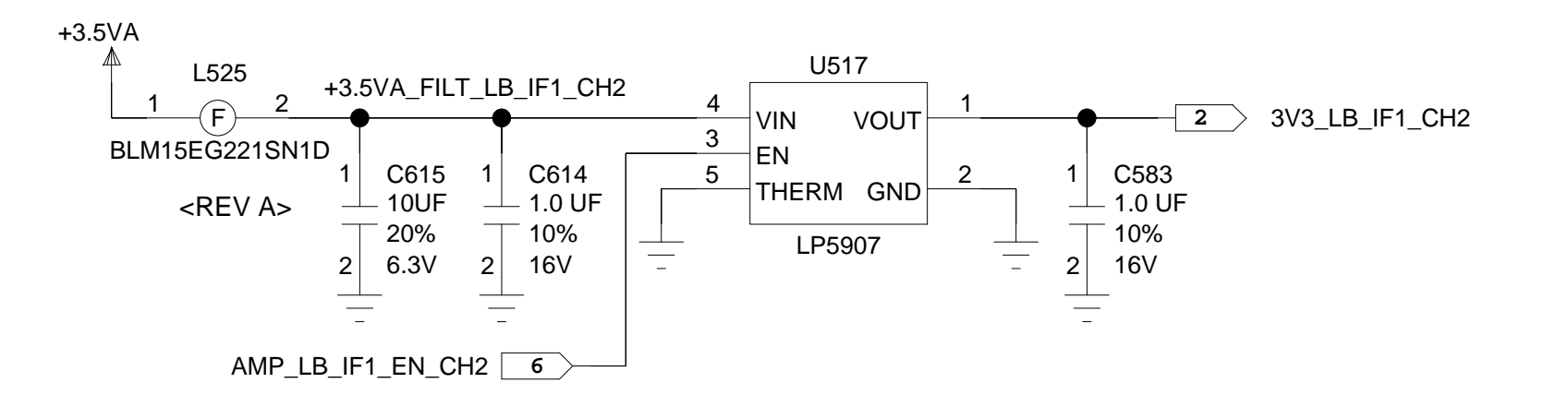
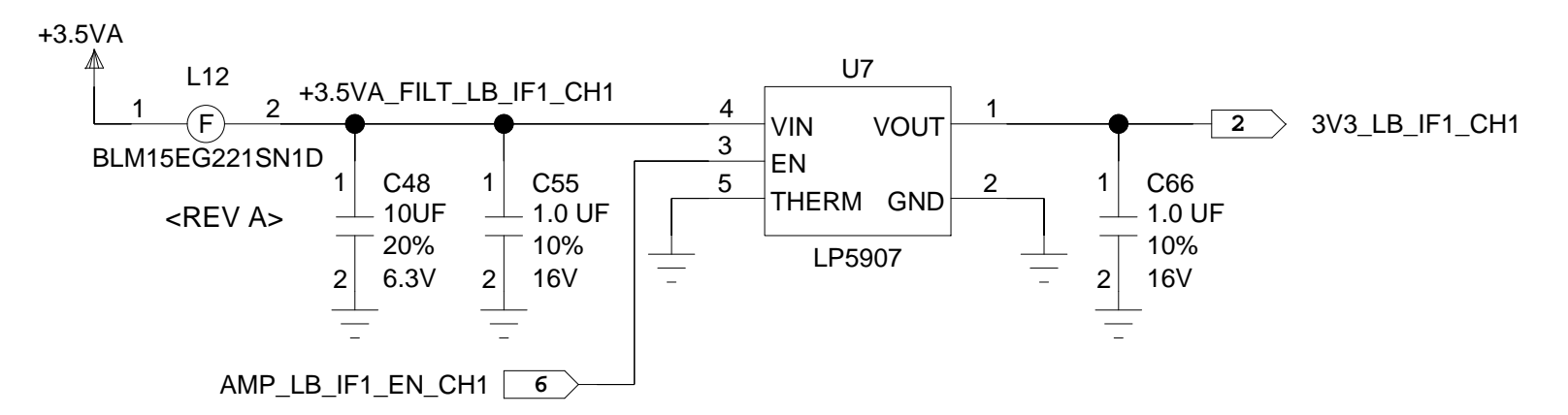
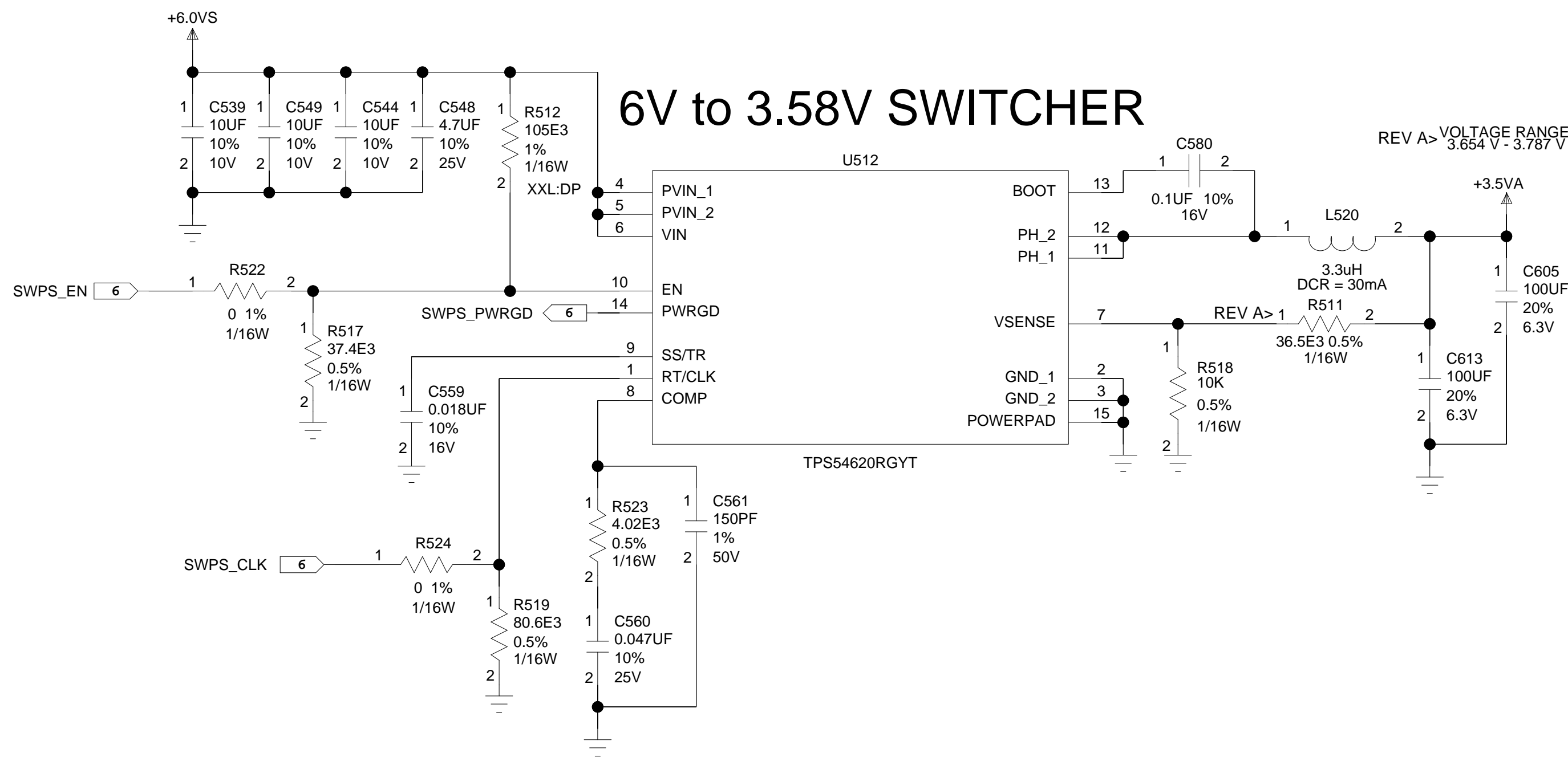
CH1 LO2 LDO: 3.58V to 3.3V



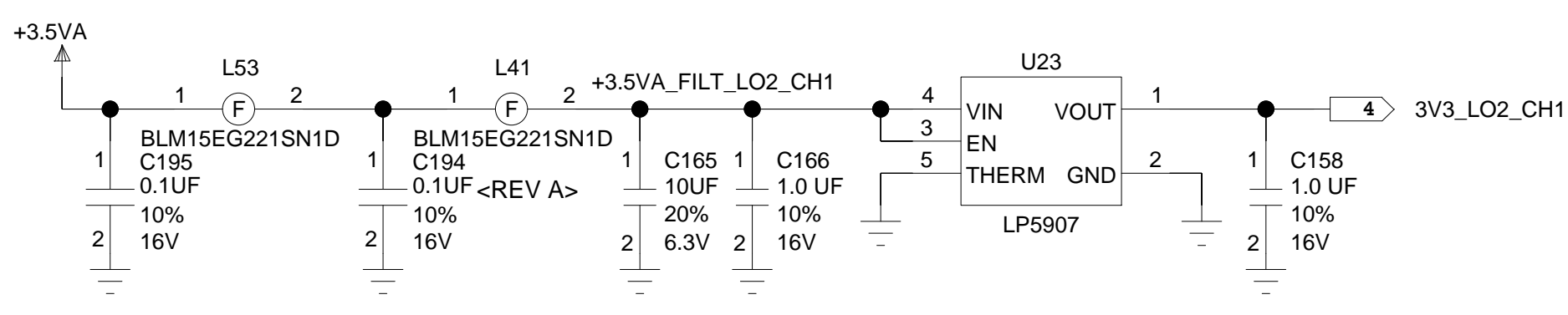
CH2 LO2 LDO: 3.58V to 3.3V



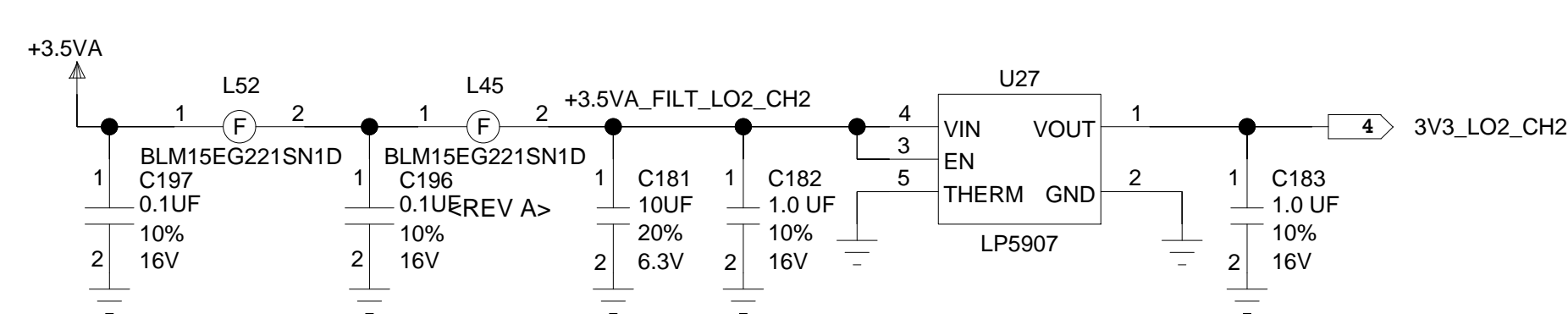
6V to 3.58V SWITCHER



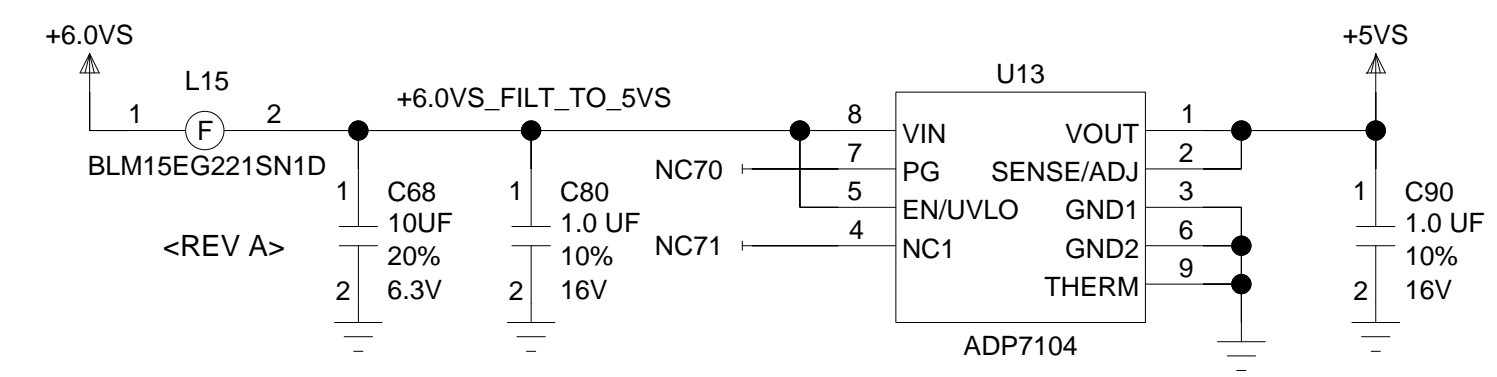
CH1 LO2 LDO: 3.58V to 3.3V



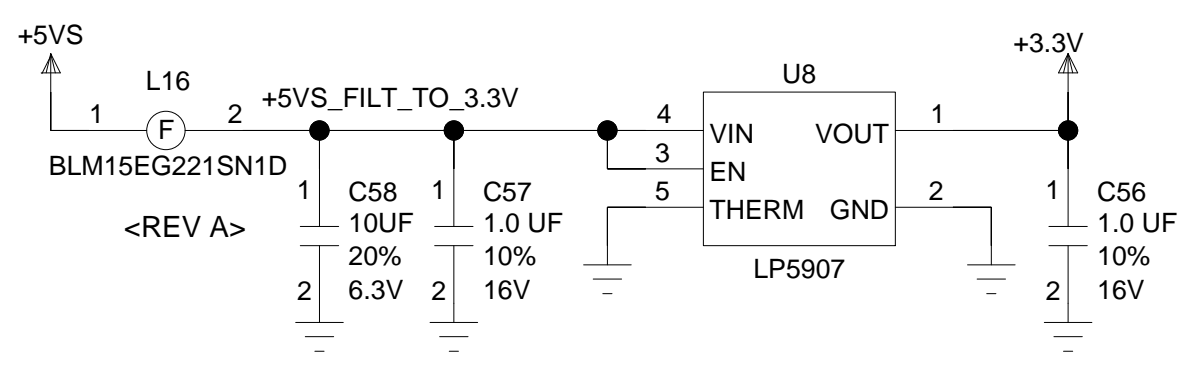
CH2 LO2 LDO: 3.58V to 3.3V



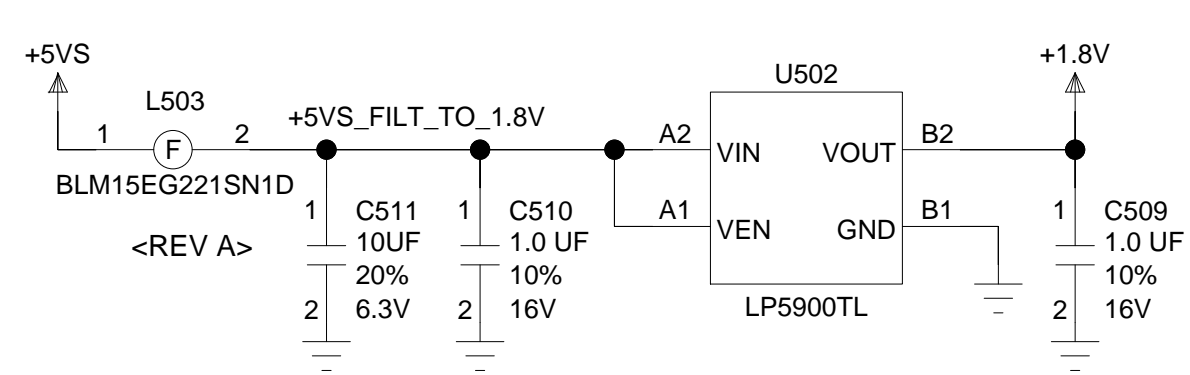
LDO: 6V to 5V



DIGITAL LDO: 5V to 3.3V



CPLD LDO: 5V to 1.8V



7-PowerSupply			
TWINRX USRP IF BD			
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