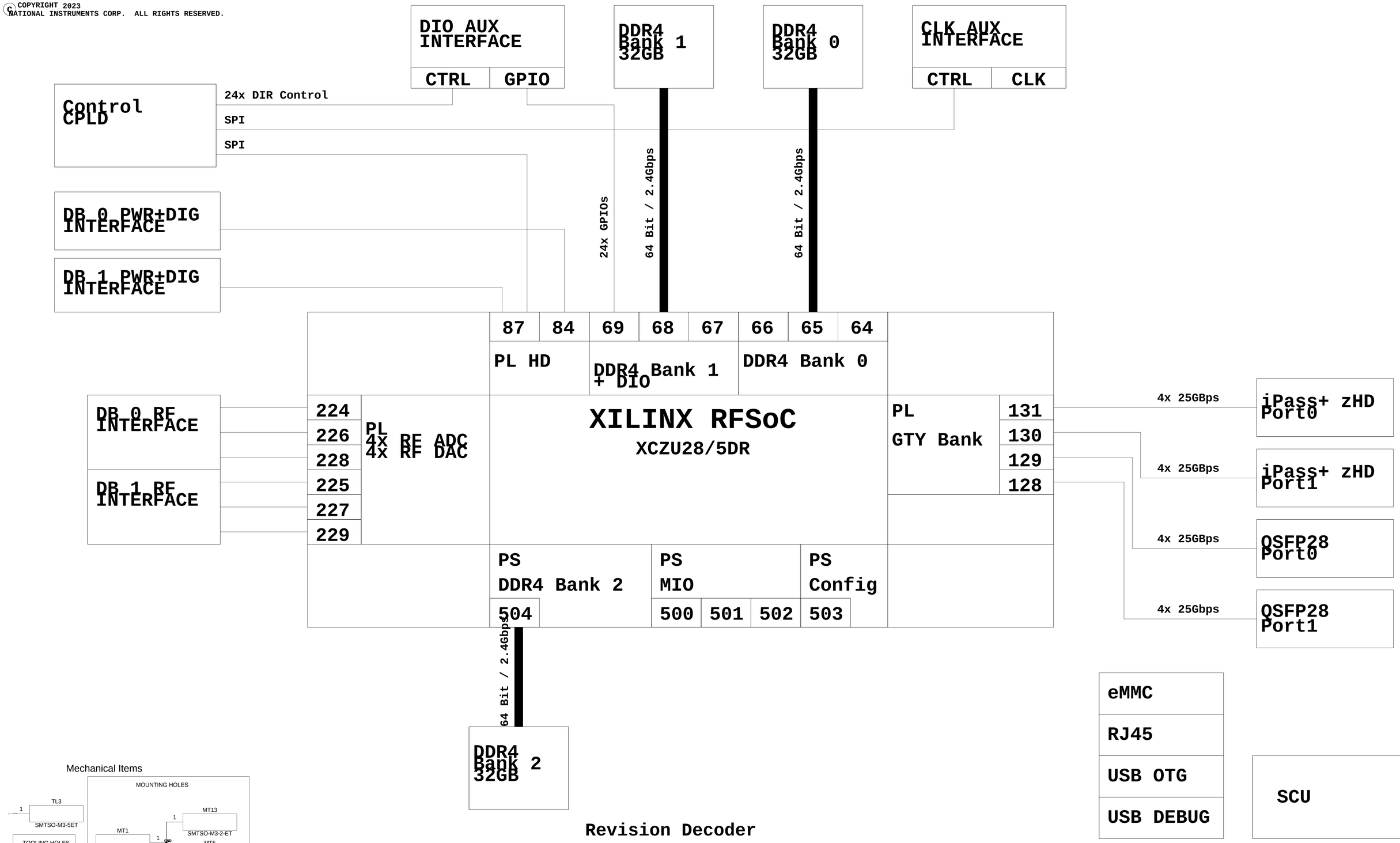
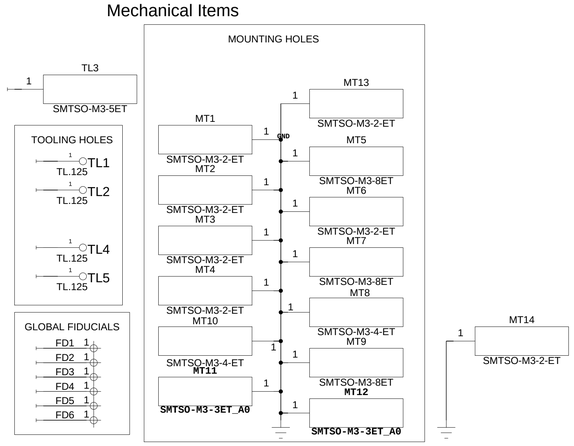
REVISIONS	
REV	DESCRIPTION
6	REFER TO DATABASE FOR DWG STATUS



Mechanical Items



Revision Decoder

Module Rev	Basecard REV	CPLD (U46)	SCU (U59)
D	E	10M04SAU169	STM32F412
E	F	10M04SAU169	STM32F411
F	G	10M08SAU169	STM32F411

DESIGN TEAM	
DRAWN	DATE
REVISED	DATE
CHECKED	
TECH	
ENGR	

NI.COM
AUSTIN, TEXAS

TITLE

SCHEMATIC DIAGRAM
USRP X410, BASECARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

SCALE: NONE

SHEET 1 OF 38

Temp Monitoring

Remote sense diode to be placed near RF FE/Amplifiers for Channel A

Remote sense diode to be placed near RF FE/Amplifiers for Channel B

Remote sense diode to be placed near the main power supply section

From FPGA sense diode

Place at TMP464

TMP464

ADC Voltages All <= 2.5V

ADC Rin = 6kOhm
ADC Cin = 4 to 7pF

Divider = 10pF
No Divider = 1000pF

2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
- The speed should not exceed 2 MHz with a maximum load of 30 pF
- These I/Os must not be used as a current source (e.g. to drive an LED)

4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

TCA9406

STM32F411VEH6

Debug Power/Reset Buttons

Combined with reset from USB JTAG to reset PS.

Fan Control and Sense

TFM-104-02-L-DH-TR

I2C Address = 0x70

I2C Address = 0x50

I2C Address = 0x68

TCA9548A

24LC024-I/MS

DS1374U-33

RTC Supercap

Fan Protection (890mA Limit)

Auto On - Low Side Gated

Floating=30V/ms

89k/100k = 890mA Limit

I2C Address = 0x20

I2C Address = 0x20

debug header

I2C Address = 0x48

I2C Addr = 0x68, 0x50

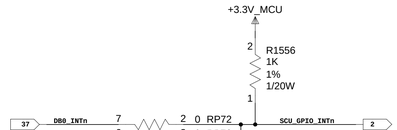
I2C Address = 0x??

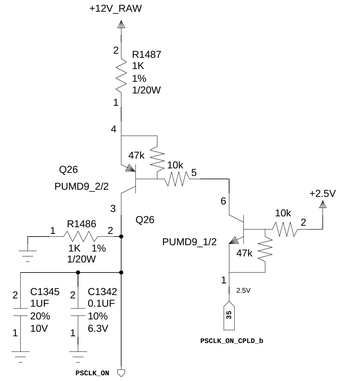
R&D Debug Header

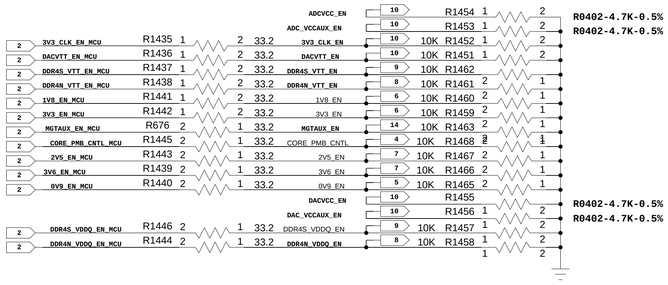
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6
SCALE: NONE		SHEET 2 OF 38	

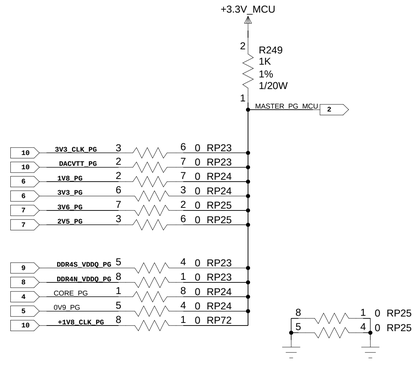
System Controller

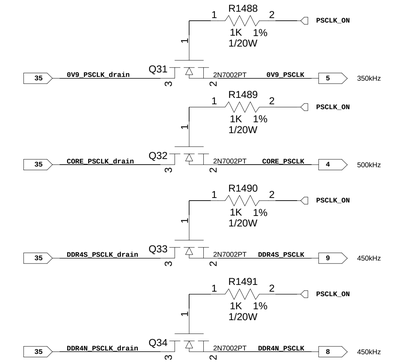
USRP X410, BASECARD

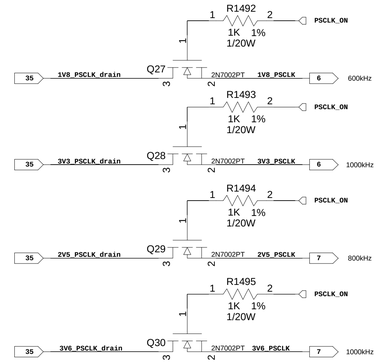


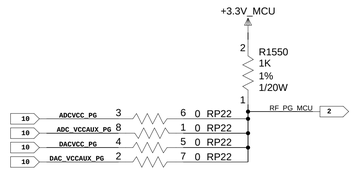




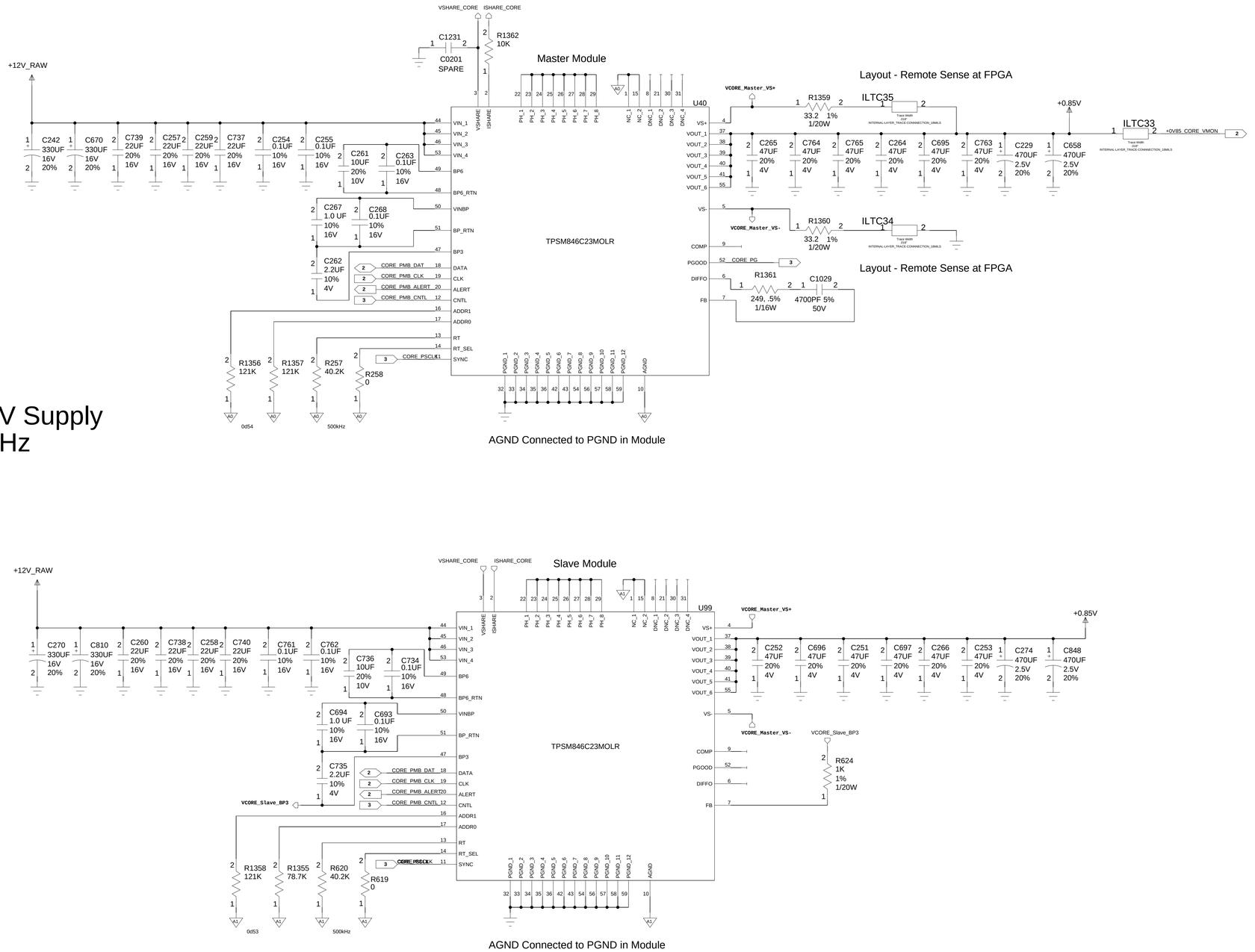






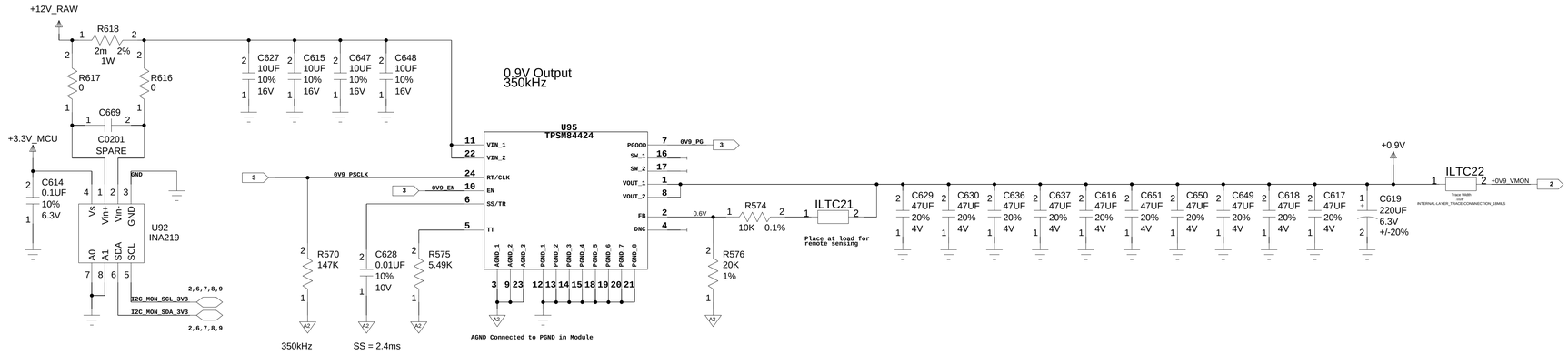


Power Control/Monitoring			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 3 OF 38	



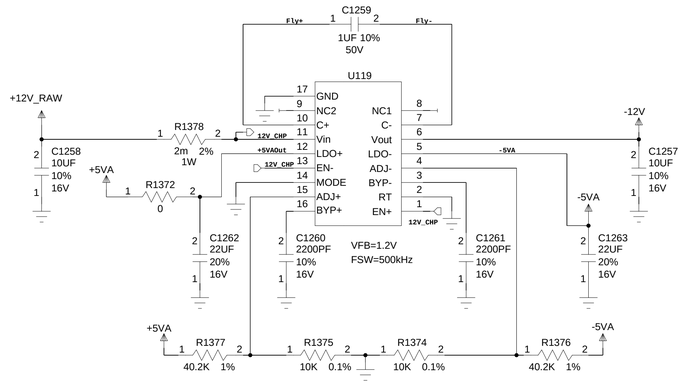
RFSoC 0.85V Supply
70A @ 500kHz

RFSoC +0V85 Core Power Supply			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE			SHEET 4 OF 38

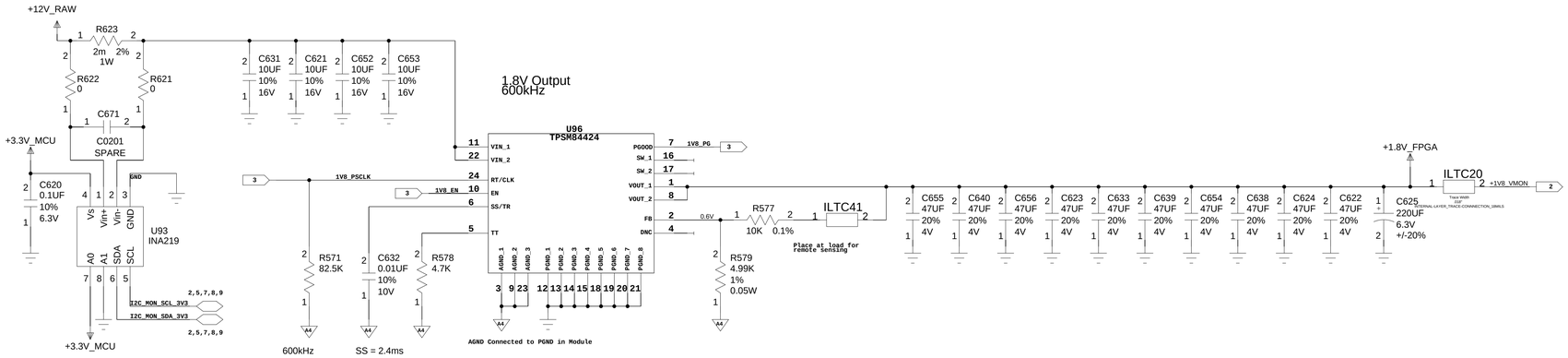


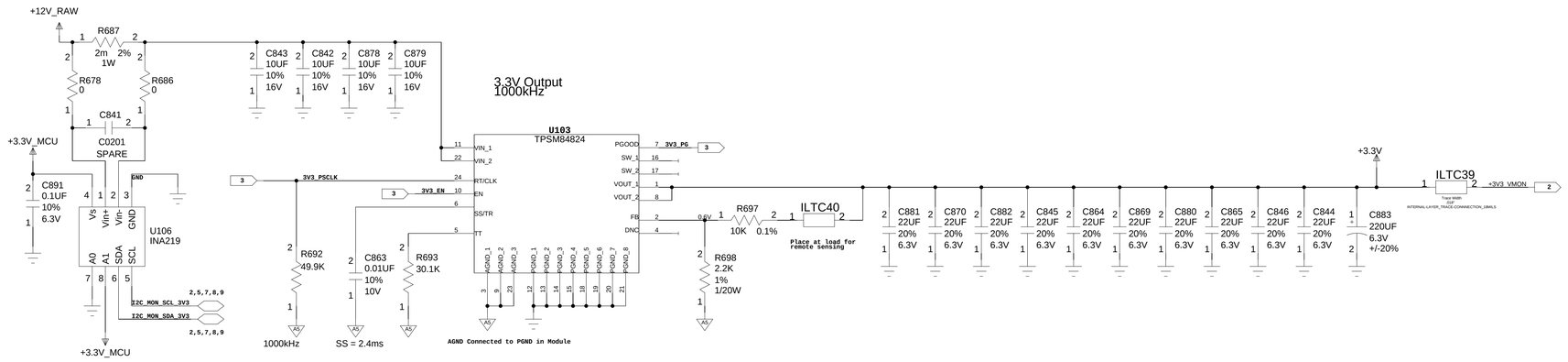
-12V Charge Pump

+5/-5V Clocking Bias



+0V9 and -12V0 Switching Supplies			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE			SHEET 5 OF 38





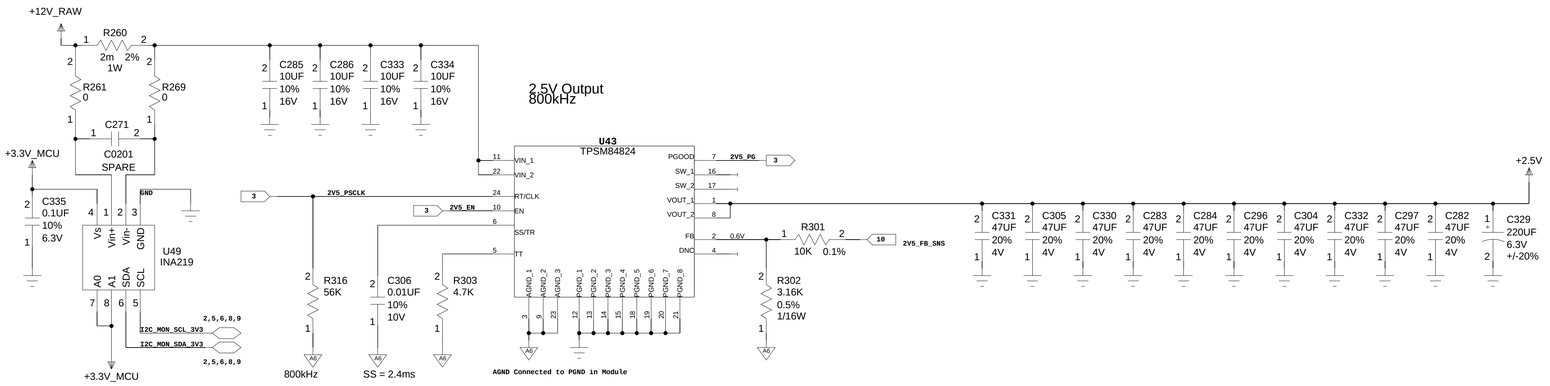
+1V8 and +3V3 Switching Supplies

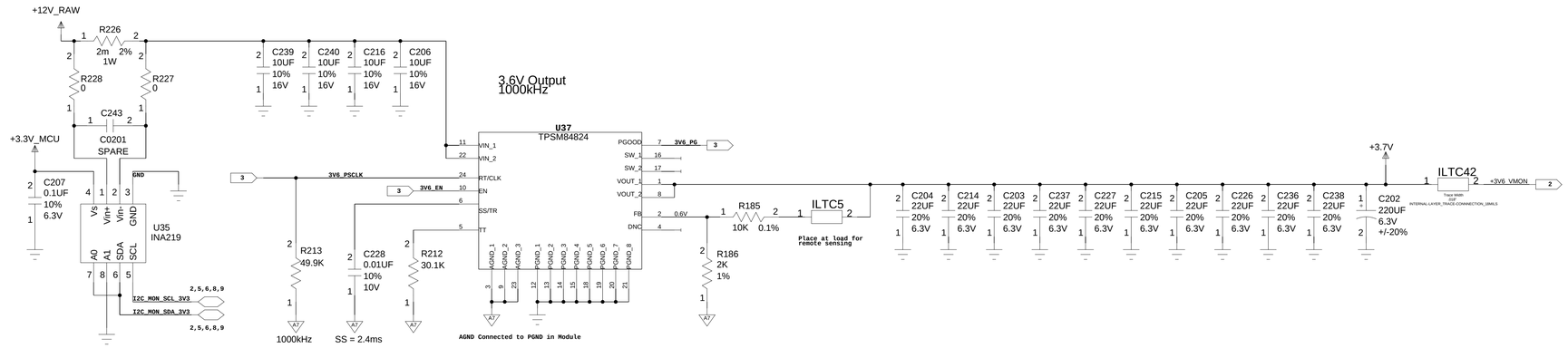
USRP X410, BASECARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

SCALE: NONE

SHEET 6 OF 38





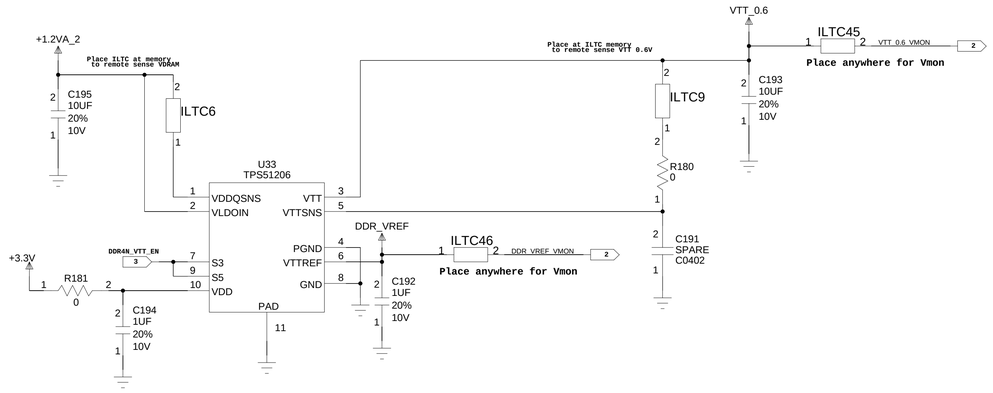
+3V6 and +2V5 Switching Supplies

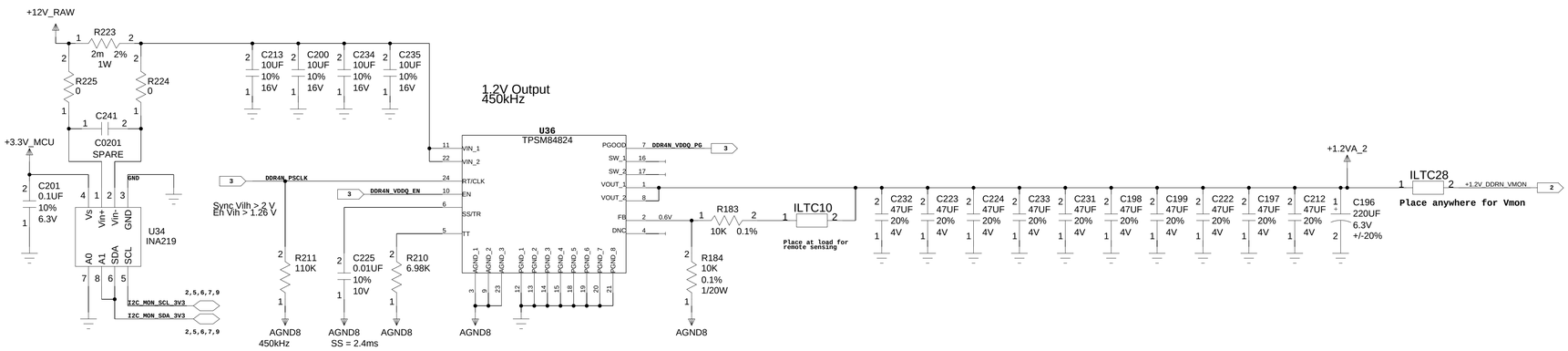
USRP X410, BASECARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

SCALE: NONE

DDR4 VTT Source/Sink LDO

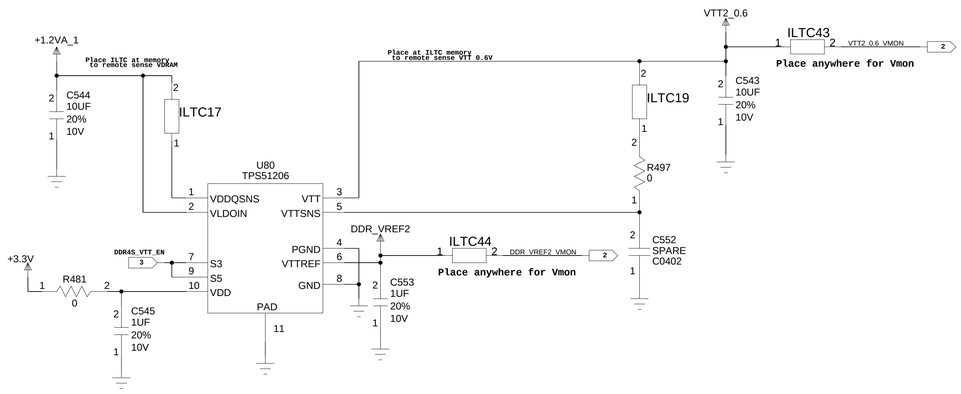


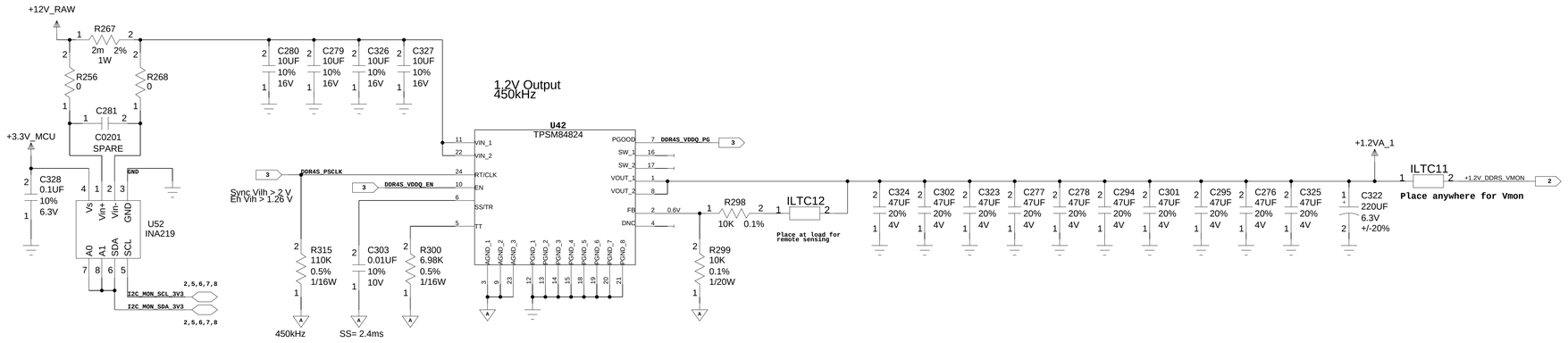


AGND Connected to PGND in Module

DDR4 and +1V2 North Power			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE			SHEET 8 OF 38

DDR4 VTT Source/Sink LDO

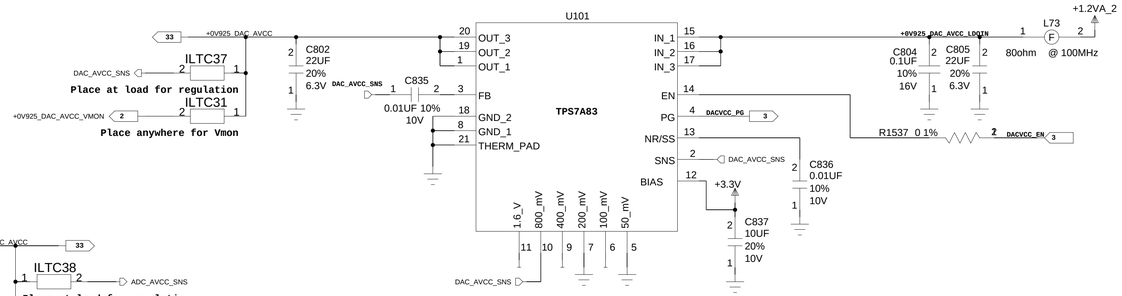




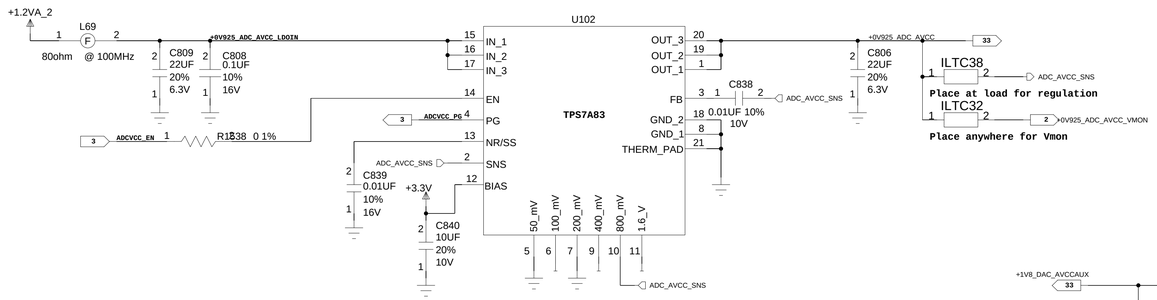
AGND Connected to PGND in Module

DDR4 and +1V2 South Power			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE			SHEET 9 OF 38

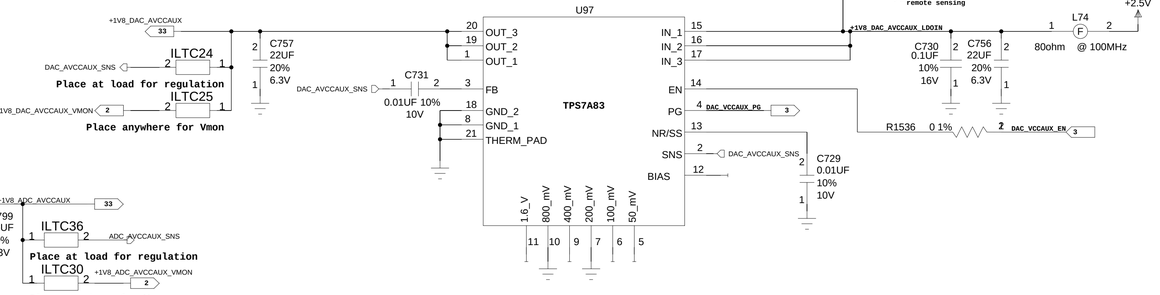
RFSoC DAC VCC 925mV +/-2% tolerance



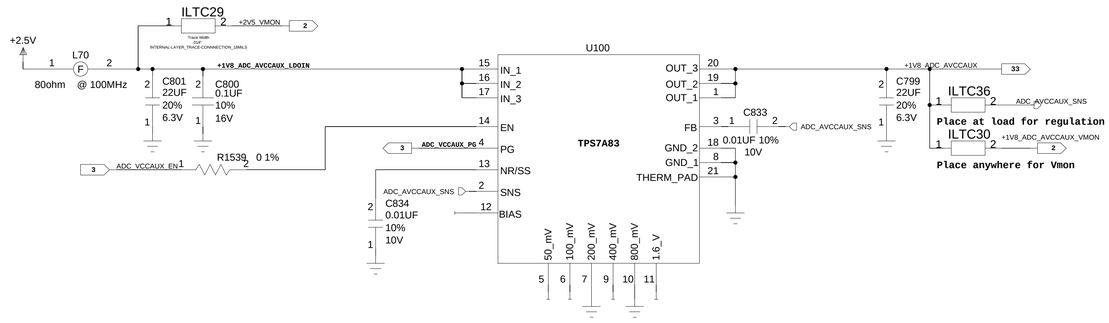
RFSoC ADC VCC 925mV +/-2% tolerance



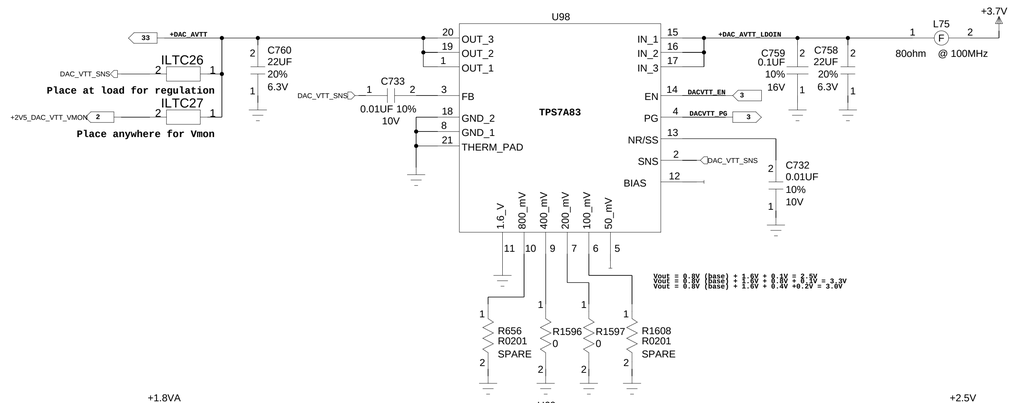
RFSoC DAC VCCAUX 1.8V +/-2% tolerance



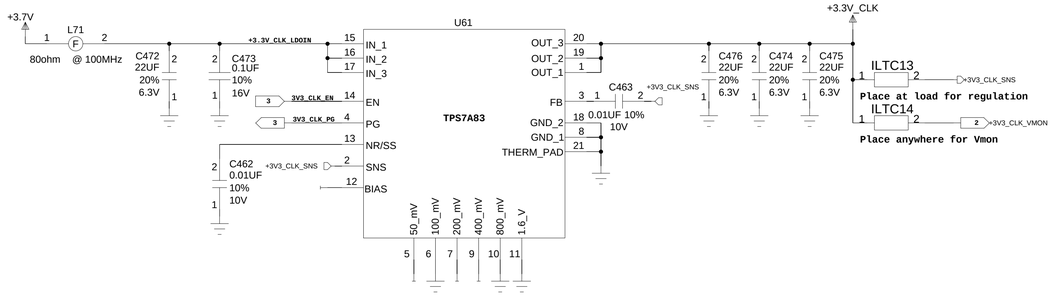
RFSoC ADC VCCAUX 1.8V +/-2% tolerance



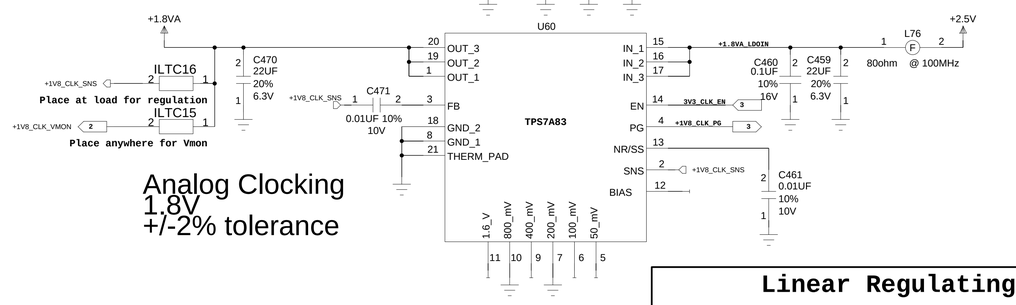
RFSoC DAC VTT 3.3V/3.0V/2.5V +/-2% tolerance



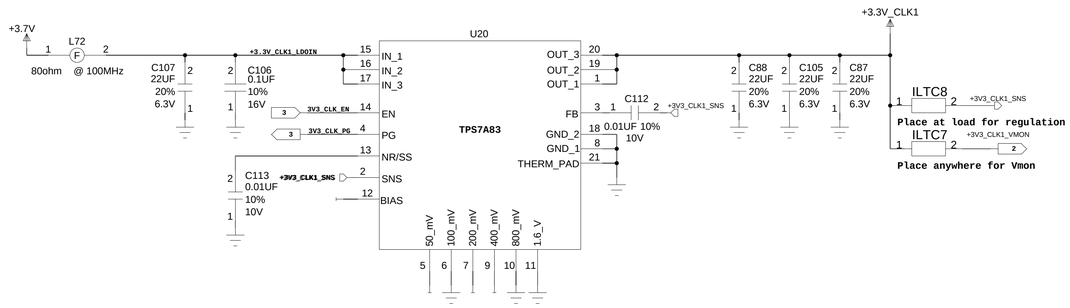
Analog Clocking 3.3V +/-2% tolerance



Analog Clocking 1.8V +/-2% tolerance



Analog Clocking 3.3V +/-2% tolerance

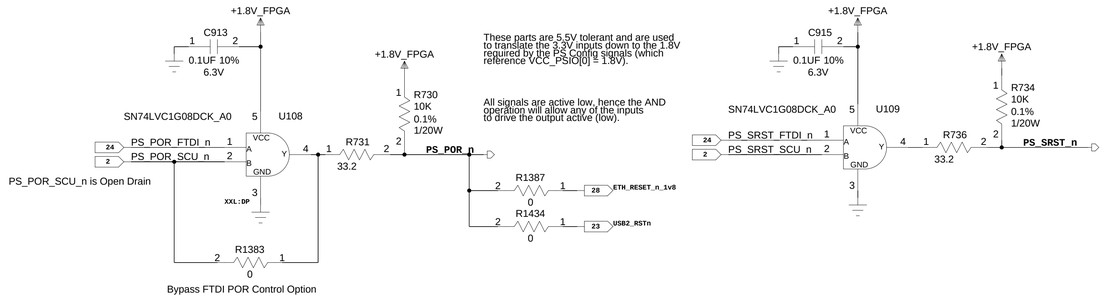


Linear Regulating Supplies

USRP X410, BASECARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

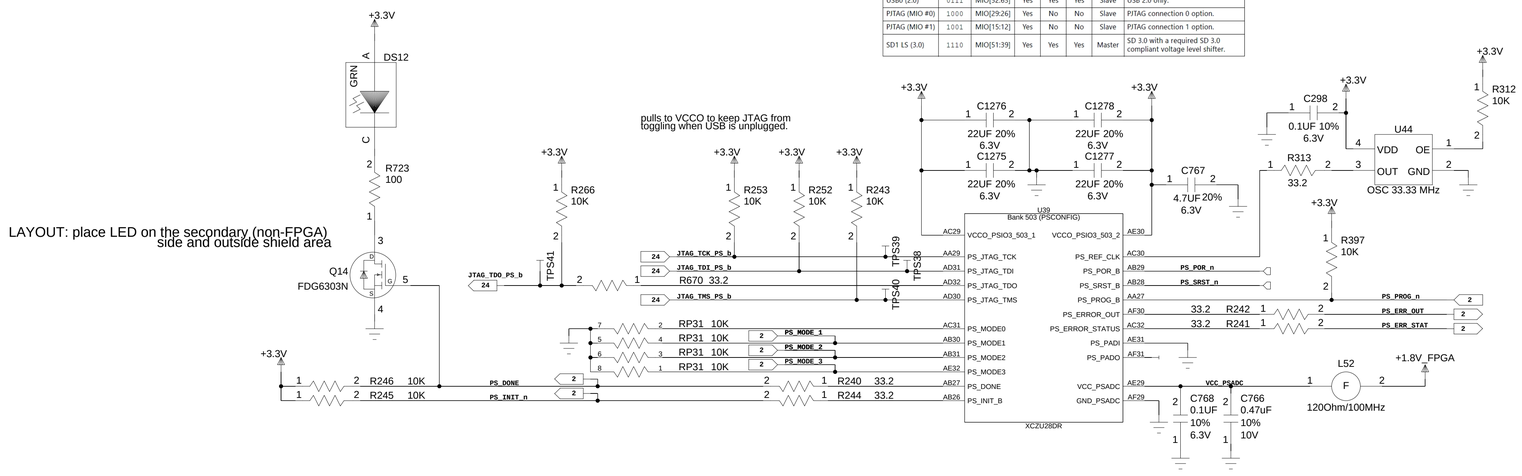
SCALE: NONE

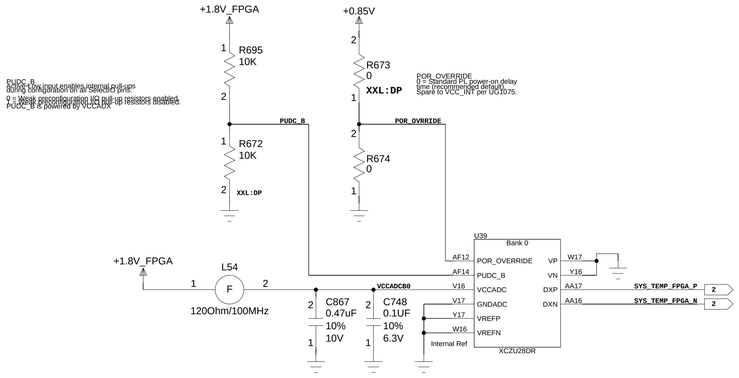


Primary boot mode is JTAG. SCU will pull these lines after it is programmed to boot from eMMC.

Table 11-1: **Boot Modes**

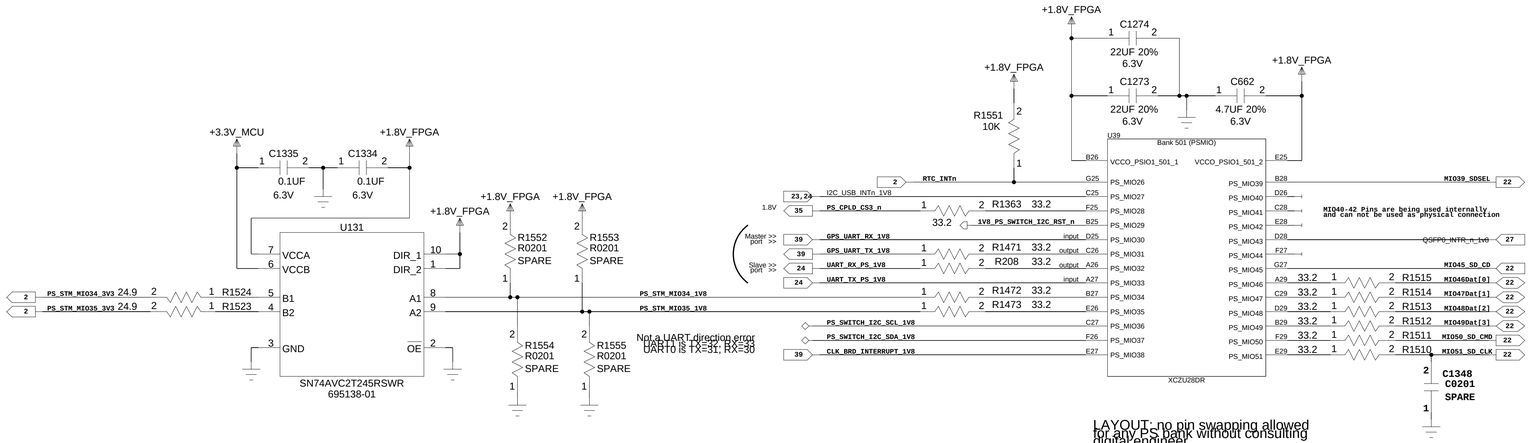
Boot Mode	Mode Pins [3:0]	Pin Location	Non-Secure	Secure	Signed	CSU Mode	Description
PS JTAG	0000	JTAG	Yes	No	No	Slave	PS/JTAG interface, PS dedicated pins.
Quad-SPI (24b)	0001	MIO[12:0]	Yes	Yes	Yes	Master	24-bit addressing (QSPI24).
Quad-SPI (32b)	0010	MIO[12:0]	Yes	Yes	Yes	Master	32-bit addressing (QSPI32).
SD0 (2.0)	0011	MIO[25:13]	Yes	Yes	Yes	Master	SD 2.0.
NAND	0100	MIO[25:09]	Yes	Yes	Yes	Master	Requires 8-bit data bus width.
SD1 (2.0)	0101	MIO[51:46]	Yes	Yes	Yes	Master	SD 2.0.
eMMC (1.8V)	0110	MIO[22:13]	Yes	Yes	Yes	Master	eMMC version 4.5 at 1.8V.
USB0 (2.0)	0111	MIO[52:63]	Yes	Yes	Yes	Slave	USB 2.0 only.
PJTAG (MIO #0)	1000	MIO[29:26]	Yes	No	No	Slave	PJTAG connection 0 option.
PJTAG (MIO #1)	1001	MIO[15:12]	Yes	No	No	Slave	PJTAG connection 1 option.
SD1 LS (3.0)	1110	MIO[51:39]	Yes	Yes	Yes	Master	SD 3.0 with a required SD 3.0 compliant voltage level shifter.

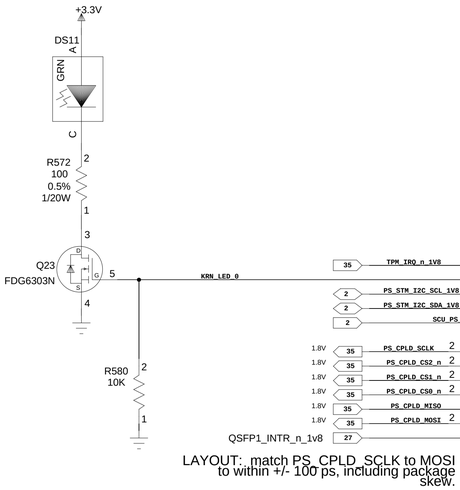


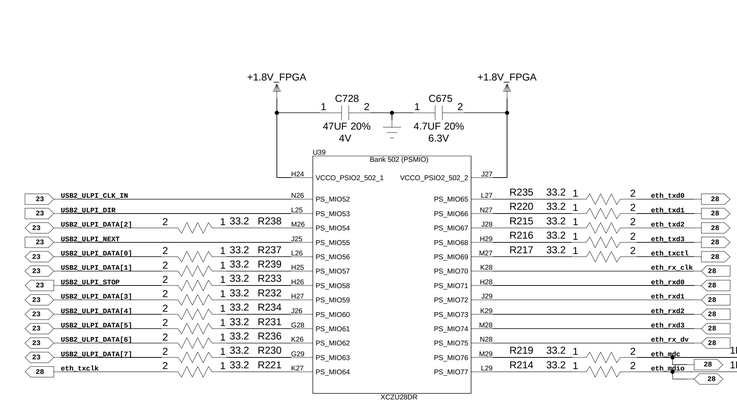


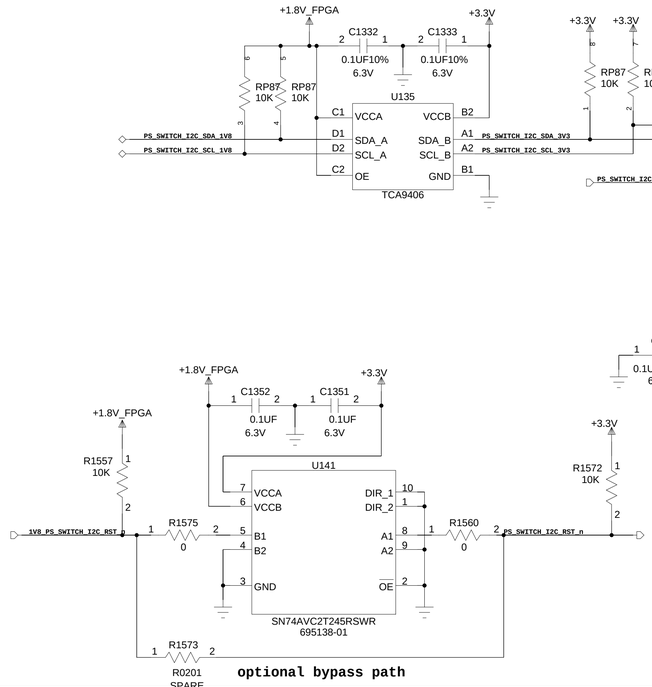
Bank 0 powered by +1.8V from VCC_AUX

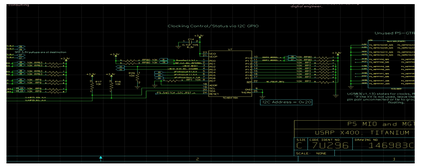
	PS Config
	USRP X410, BASECARD
SIZE: C	CODE IDENT NO.: 7U296
DRAWING NO.:	146983*-01
REV:	6
SCALE: NONE	SHEET 11 OF 38

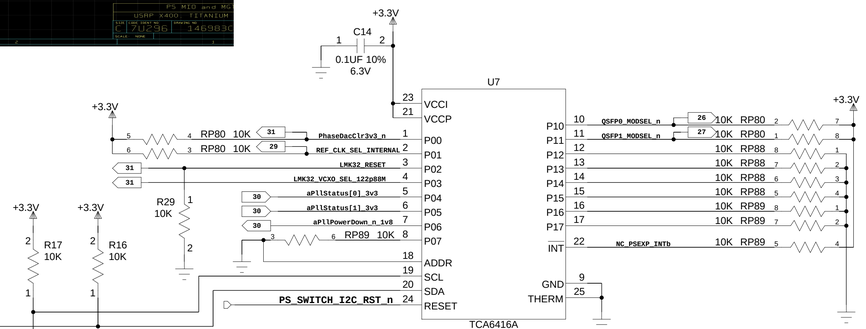


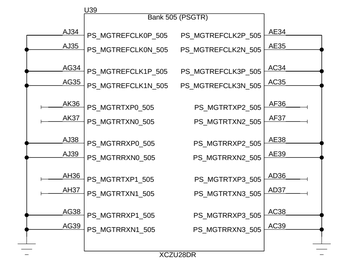








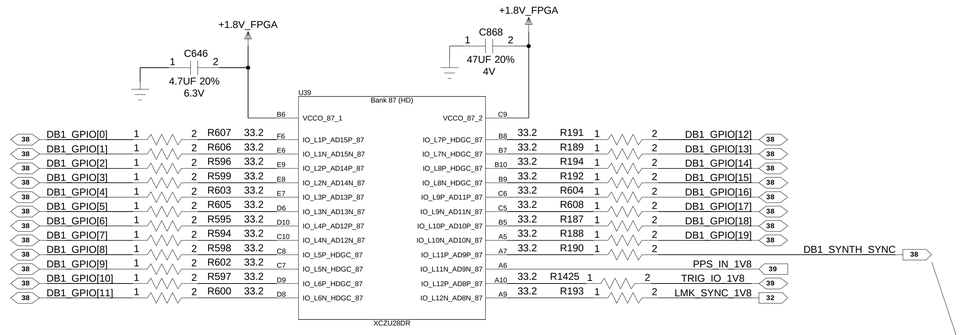




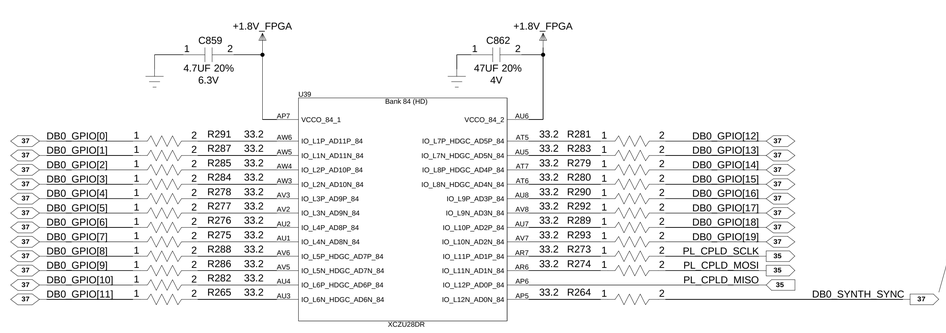
UG583(v1.13) states for clocks, RX, and TX pairs: "If the XX is not used, leave the associated pin pair unconnected or tie to ground." Leaving TX floating.

POR: All Inputs
RESET Active Low!

PS MIO and MGTs			
USRP X410, BASECARD			
SIZE C	**CODE IDENT NO.** 7U296	**DRAWING NO.** 146983*-01	**REV** 6
SCALE: NONE		**SHEET** 12 **OF** 38	



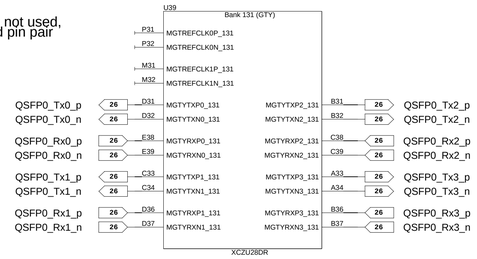
LAYOUT: any HD bank signals may be swapped.
No strict rules apply to any signals here.



LAYOUT: DB*_SYNTH_SYNC signals should be length matched within 10th, including package bond wire lengths.

PL HD			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 13 OF 38	

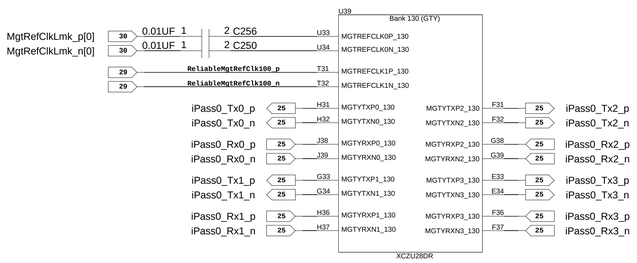
UG578:
If reference pins are not used, leave the associated pin pair unconnected



Quad 131

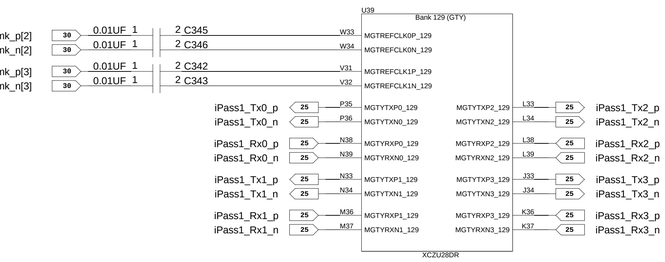
LMK03328 drives the clocks LVDS

GTY Requirements:
V_diff = [250, 2000]mV
V_cm = 0.9V (MGTAVCC)



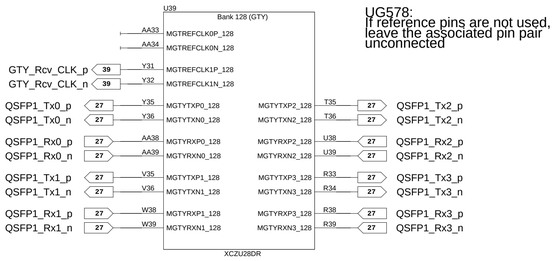
LMK03328 drives the clocks LVDS

GTY Requirements:
V_diff = [250, 2000]mV
V_cm = 0.9V (MGTAVCC)



Quad Mapping		
PCIe x8	Quad	Connector
	Bank 131	QSFP28 0
	Bank 130	iPass+zHD 1
	Bank 129	iPass+zHD 0
	Bank 128	QSFP28 1

UG578:
If reference pins are not used, leave the associated pin pair unconnected



Quad 128

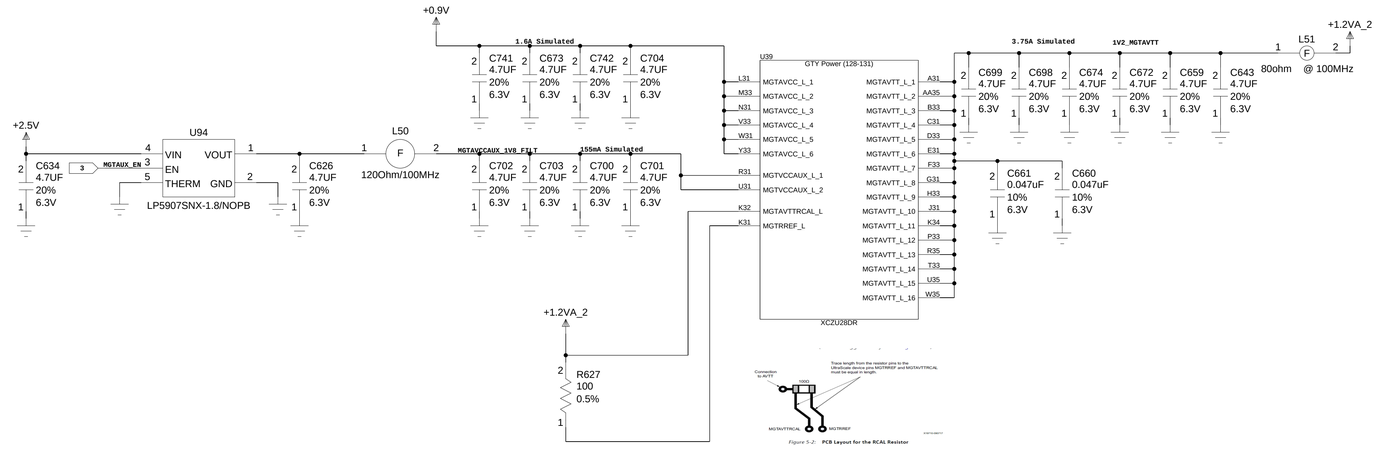


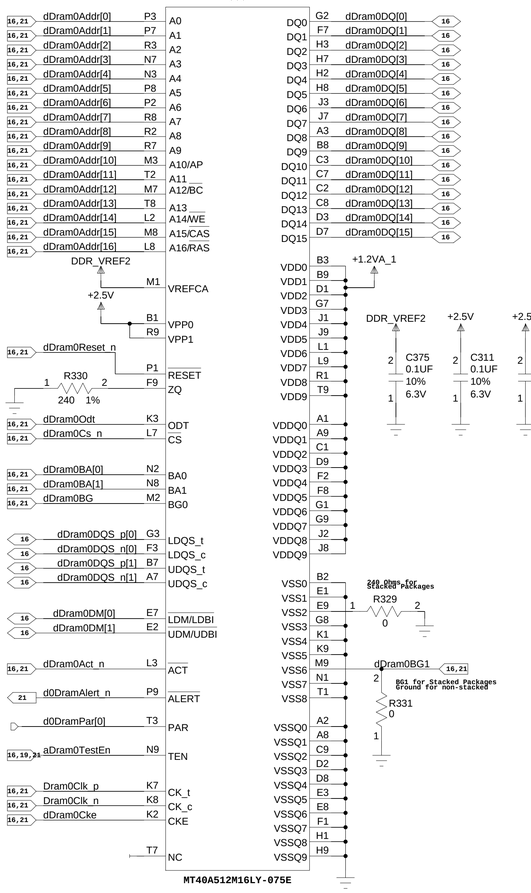
Figure 5-2: **PCB Layout for the RCAL Resistor**

Table 5-4: **GTY Transceiver PCB Capacitor Recommendations**

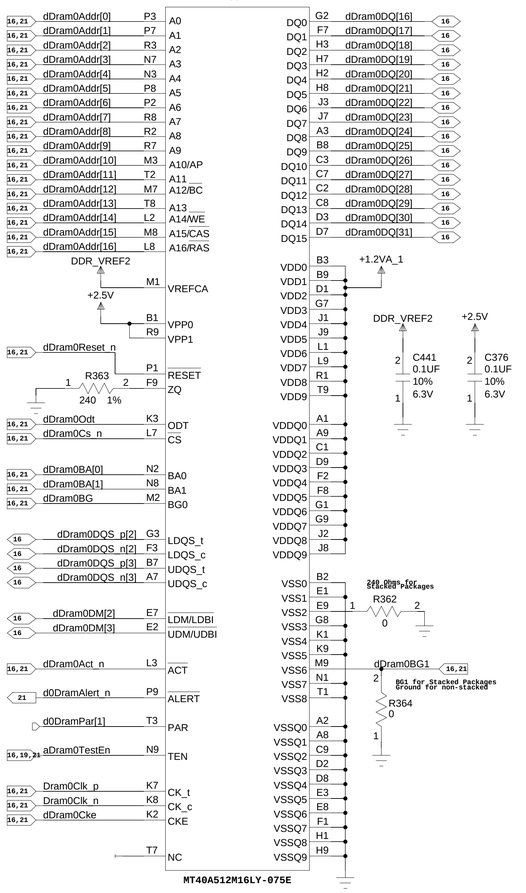
Quantity Per Group			Capacitance (µF)	Tolerance	Type
MGTAVCC	MGTAVTT	MGTVCCAUX			
1	1	1	4.70	±10%	Ceramic

PL MGTs	
USRP X410, BASECARD	
SIZE: **C**	CODE IDENT NO.: **7U296**
DRAWING NO.: **146983*-01**	REV: **6**
SCALE: **NONE**	SHEET **14** OF **38**

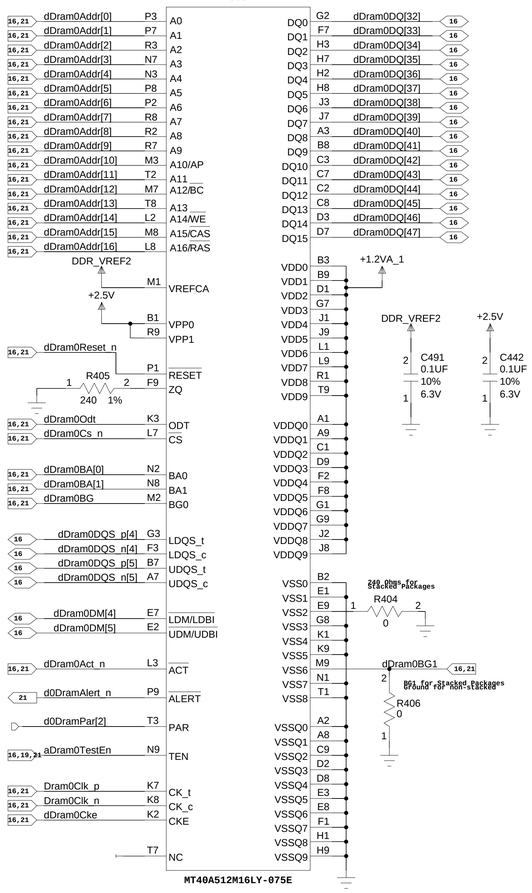
U50



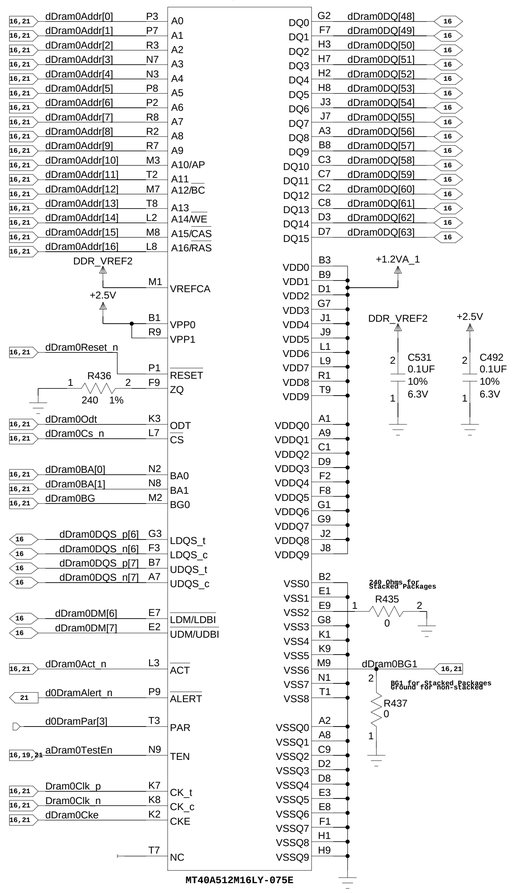
U57



U63



U71



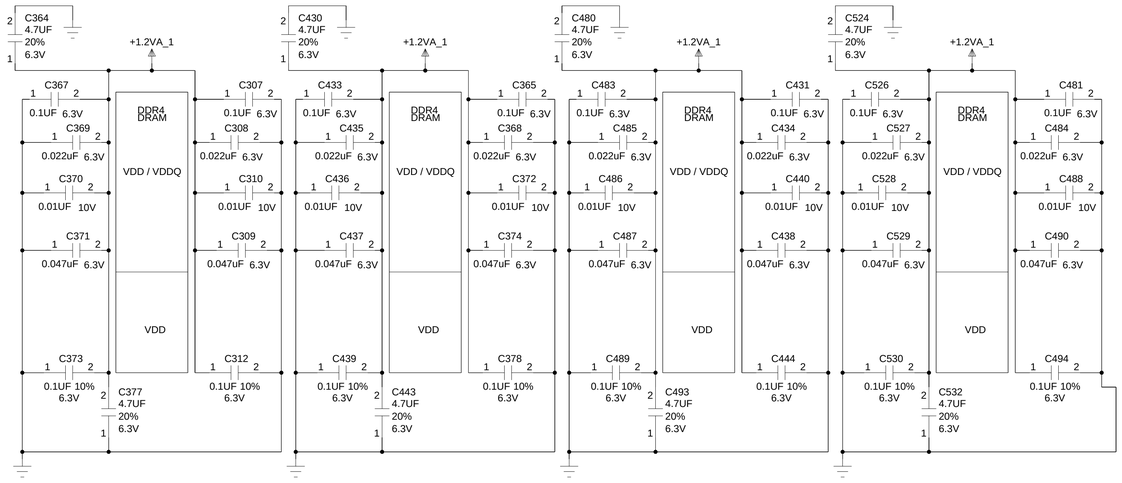
d0DramPar[0]
R355 10K

d0DramPar[1]
R380 10K

d0DramPar[2]
R423 10K

d0DramPar[3]
R453 10K

DDR4 Decoupling Cap Placement



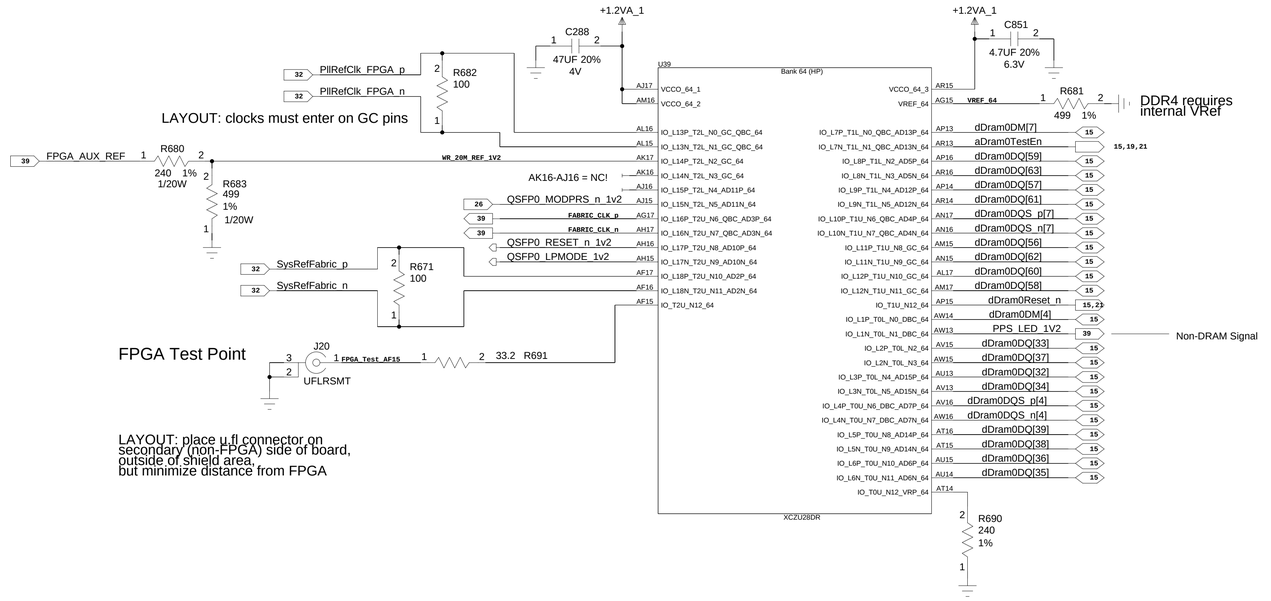
PL DDR4 Bank 0 South

USRP X410, BASECARD

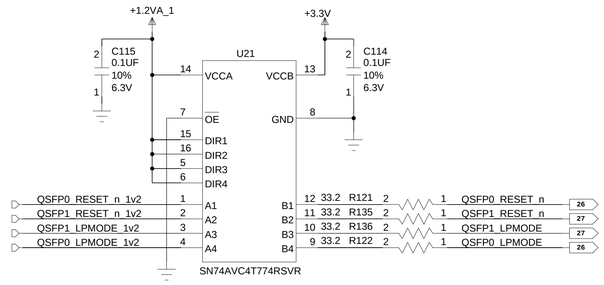
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

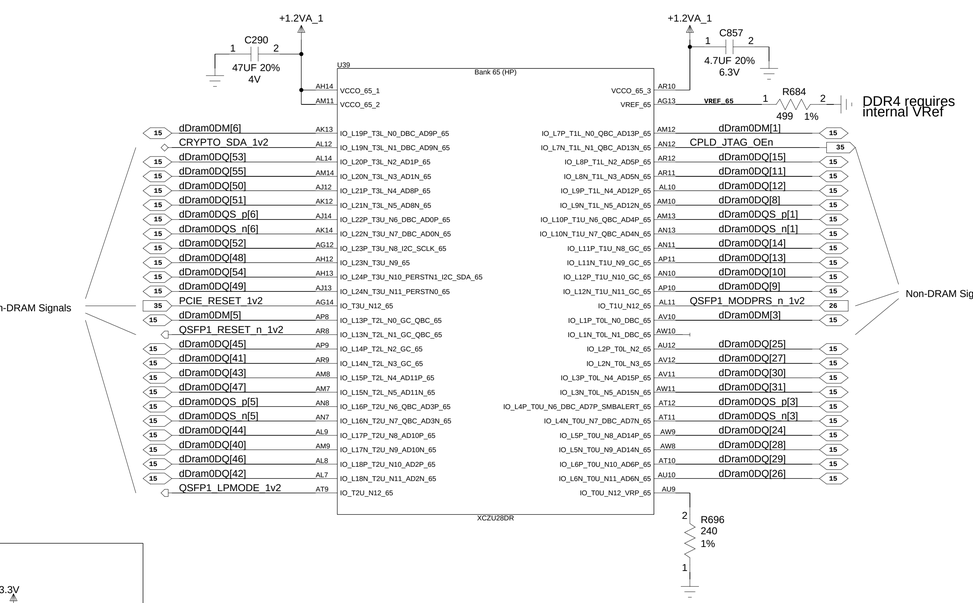
SCALE: NONE

SHEET 15 OF 38



Translation for output QSFP Sideband Signals to Connectors





Pre-programmed ATSHA204A for board authentication.

PL DRAM Bank 0 Interface

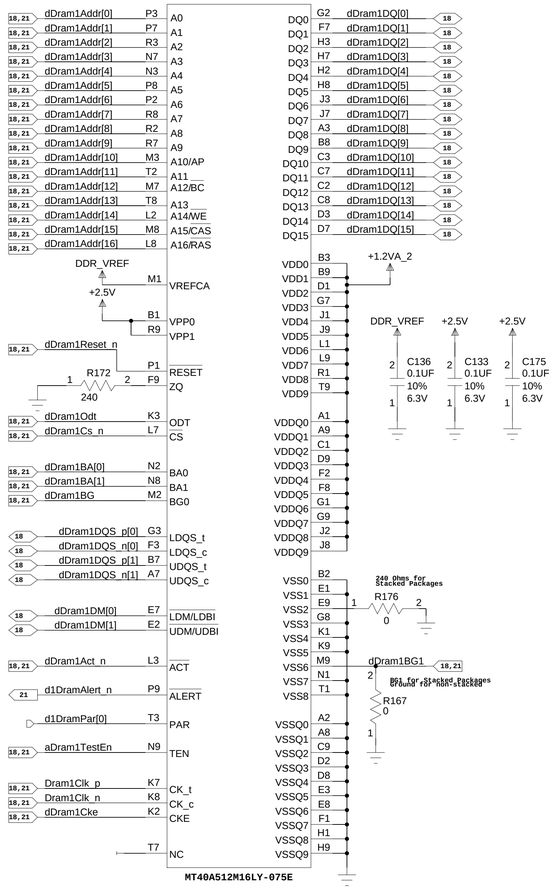
USRP X410, BASECARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

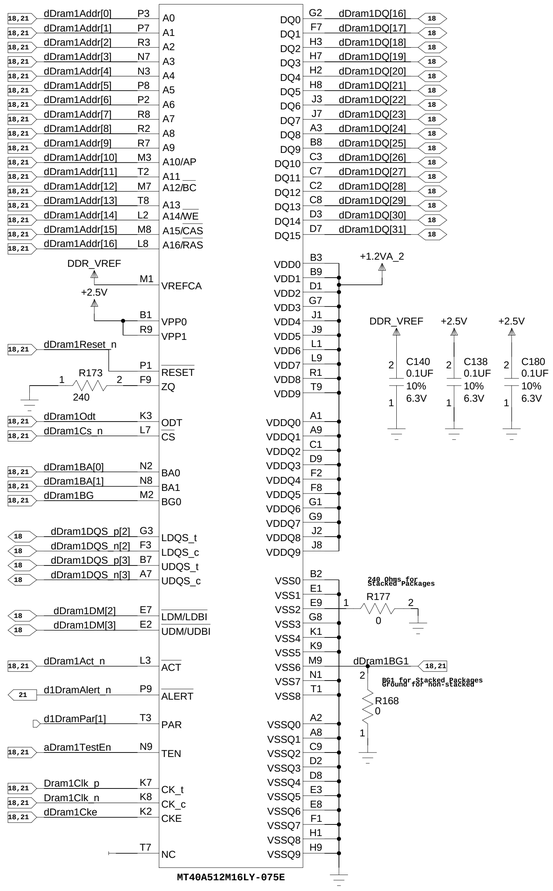
SCALE: NONE

SHEET 16 OF 38

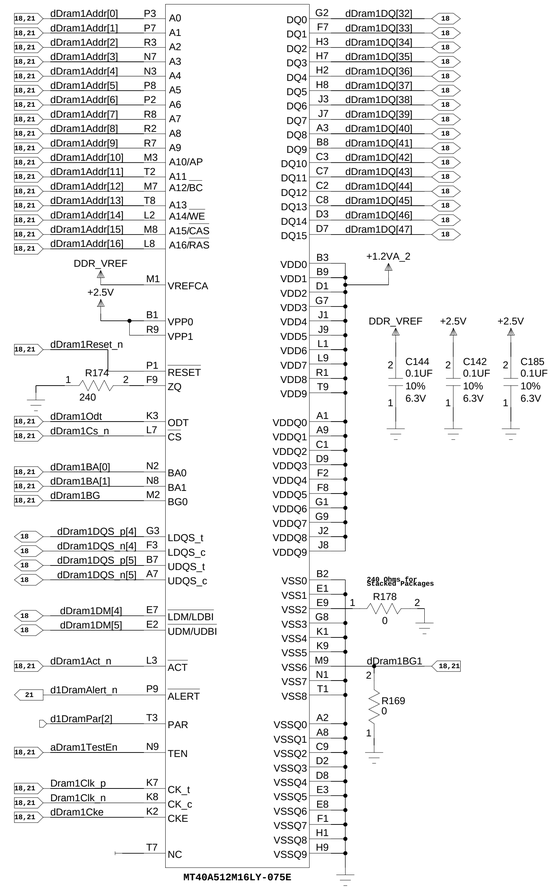
U29



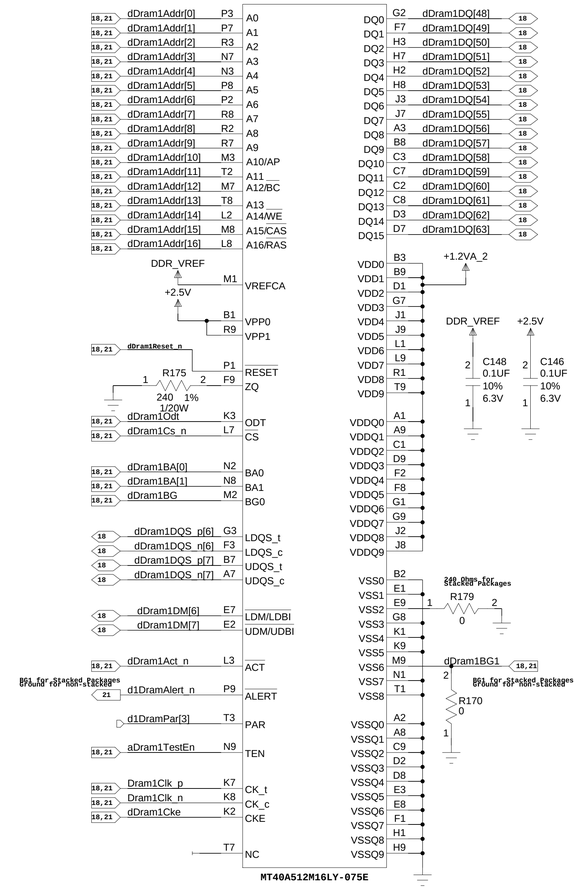
U30



U31



U32



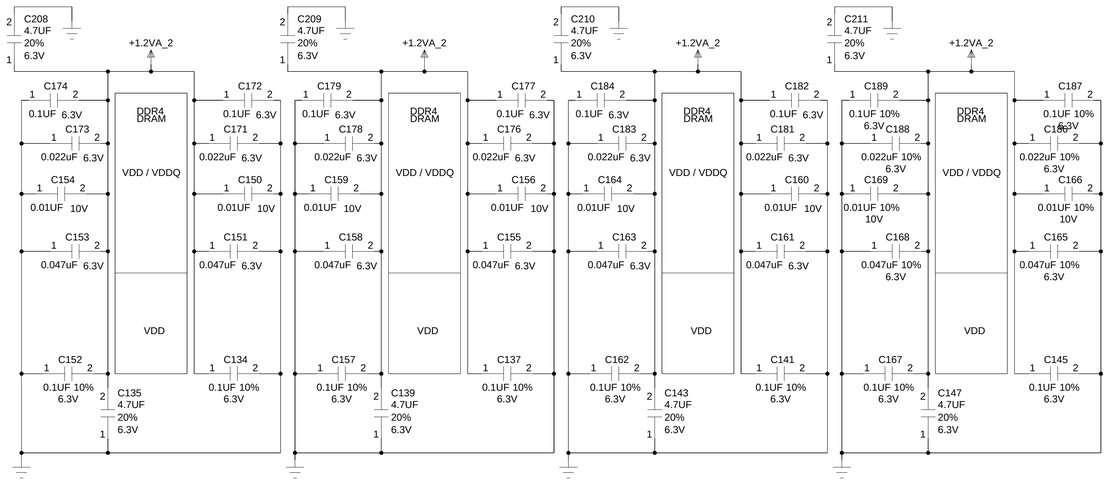
d1DramPar[0] R154 10K

d1DramPar[1] R157 10K

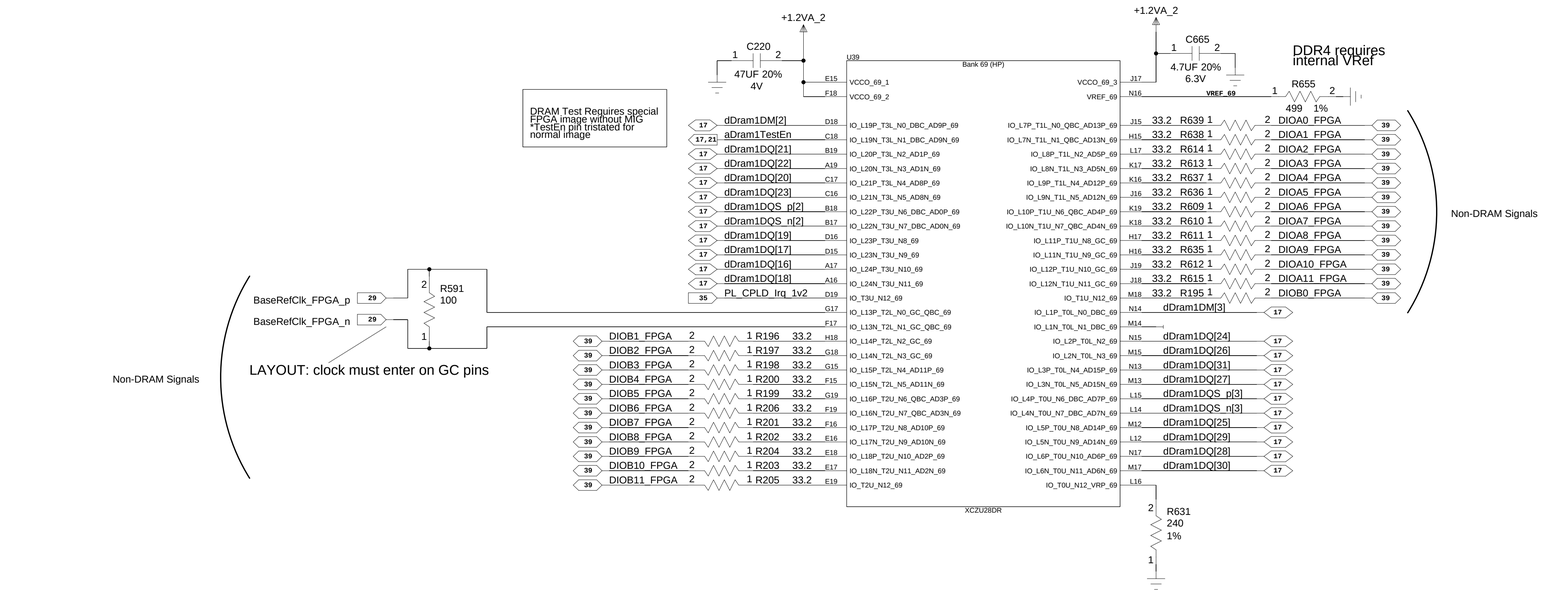
d1DramPar[2] R158 10K

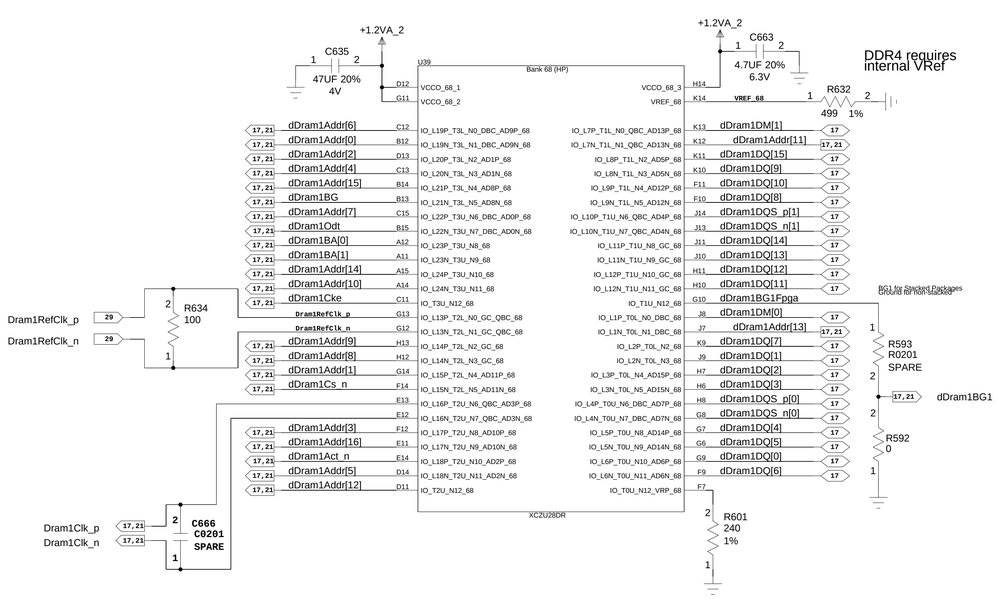
d1DramPar[3] R159 10K

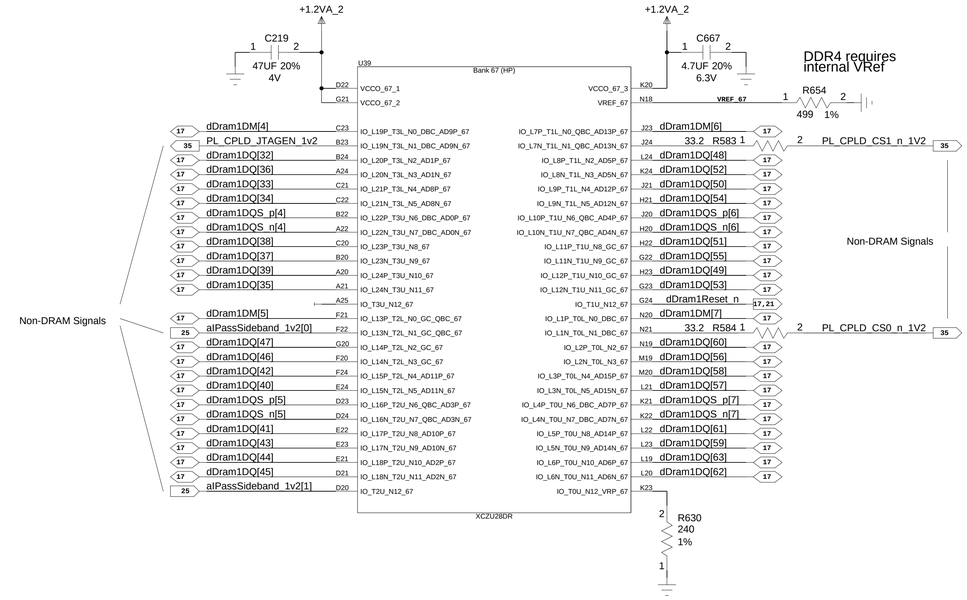
DDR4 Decoupling Cap Placement



PL DDR4 Bank 1 North			
USRP X410, BASECARD			
SIZE C	CODE IDENT NO. 7U296	DRAWING NO. 146983*-01	REV 6
SCALE: NONE		SHEET 17 OF 38	

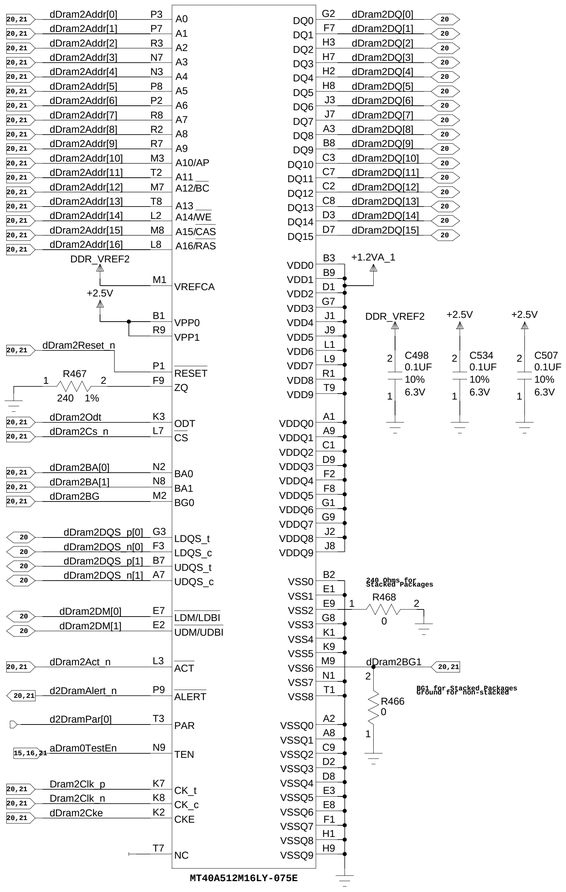




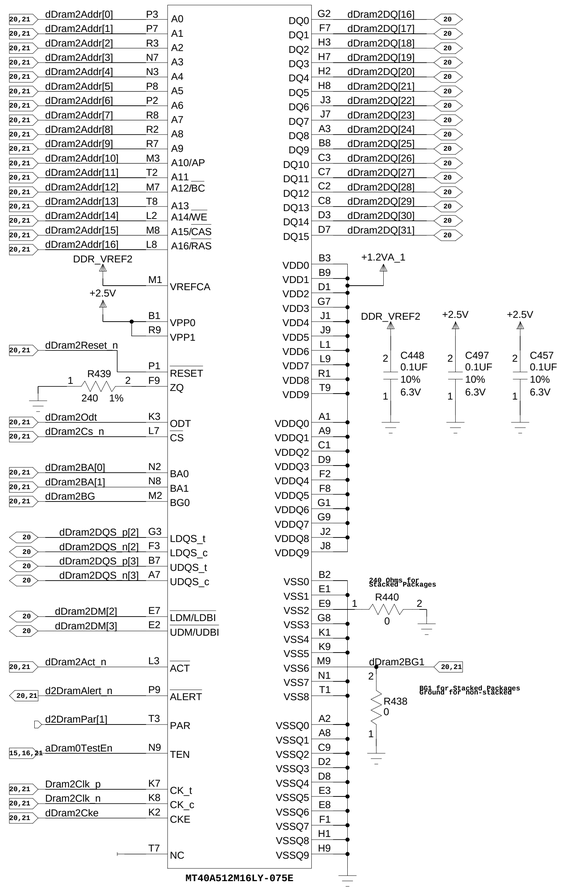


PL DRAM Bank 1 Interface And Panel DIO			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 18 OF 38	

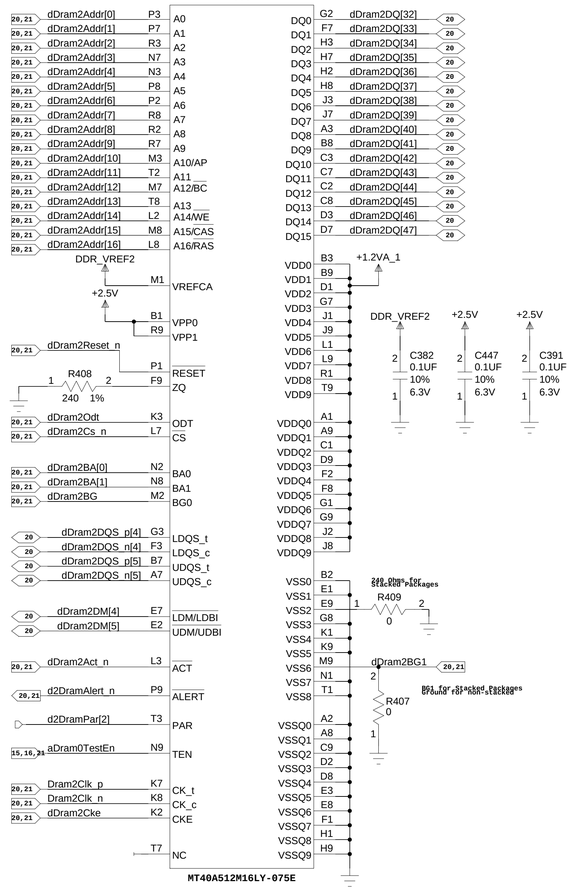
U72



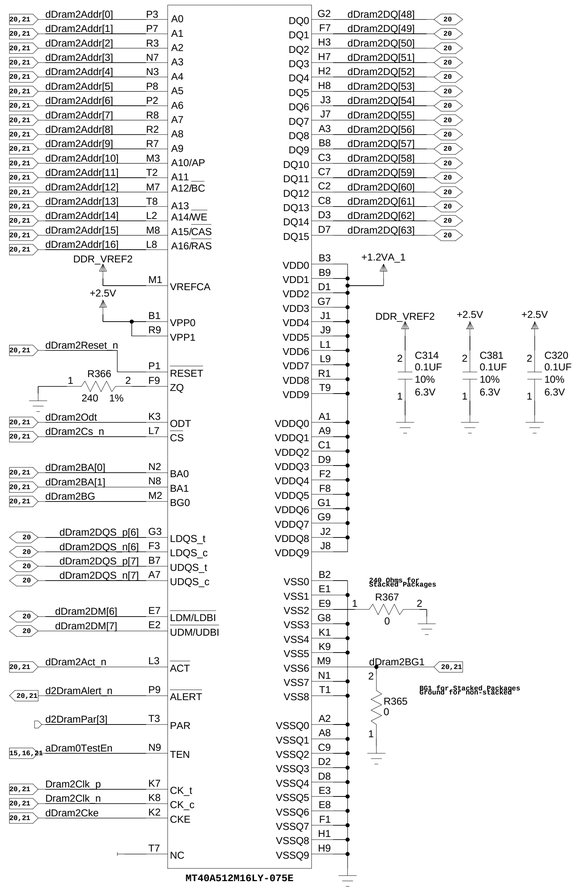
U64

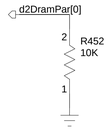


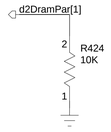
U58

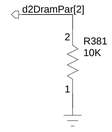


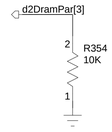
U51



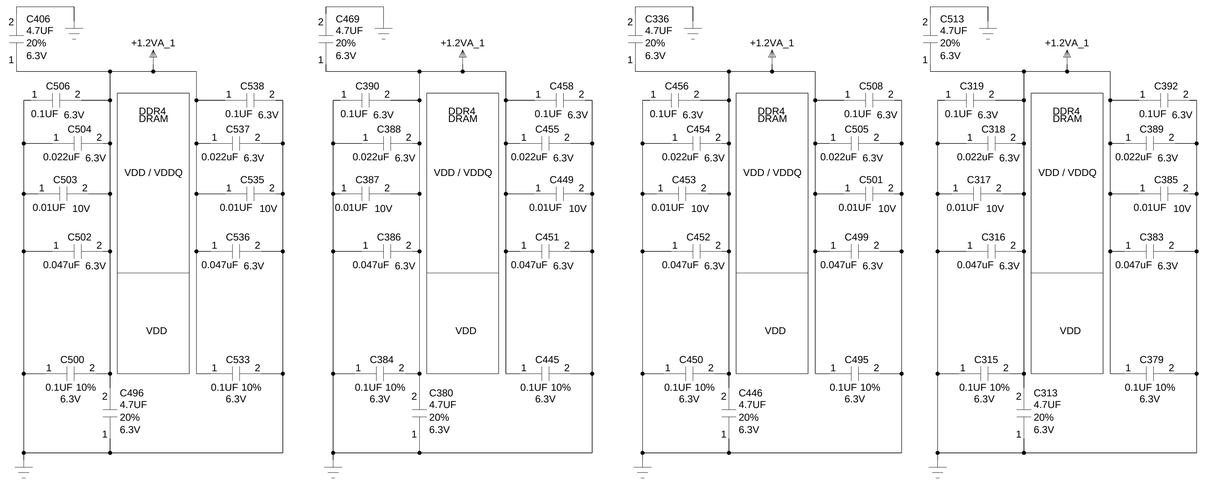




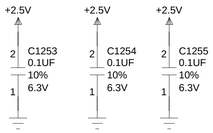




DDR4 Decoupling Cap Placement



LYR7 stitching caps

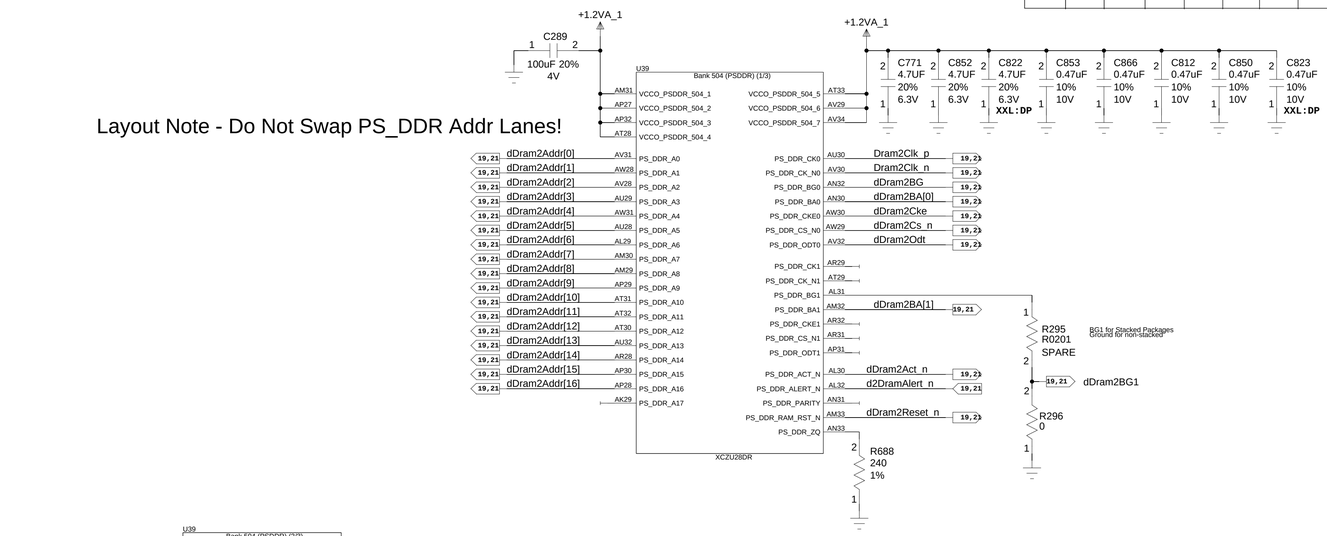


PS DDR4 Bank 2 South			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 19 OF 38	

Table 1-10: **Zynq UltraScale+ MPSoC PS Decoupling Capacitor Recommendations**

$V_{CC\_PSINTLP}$		$V_{CC\_PSINTFP}$		V_{CC_PSAUX}		V_{CC_PSPLL}		$V_{CC\_PSINTFP\_DDR}$		V_{CC_PSBATT}		V_{CCO_PSDDR}		
100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	0.47 µF
1	1	1	1	1	1	1	1	1	1	1	1	1	2	4

Layout Note - Do Not Swap PS_DDR Addr Lanes!



PS DDR4 Bank 2 Interface				
USRP X410, BASECARD				
SIZE	CODE IDENT NO.	DRAWING NO.		REV
C	7U296	146983*-01		6
SCALE: NONE			SHEET 20 OF 38	

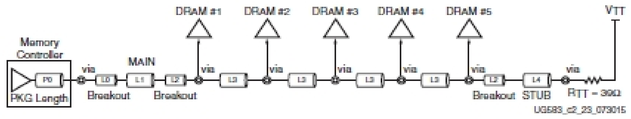


Figure 2-21: **Address, Command, and Control Fly-by Termination for DDR4 SDRAM**

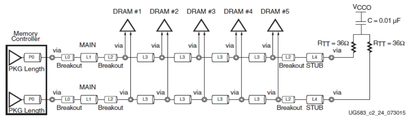
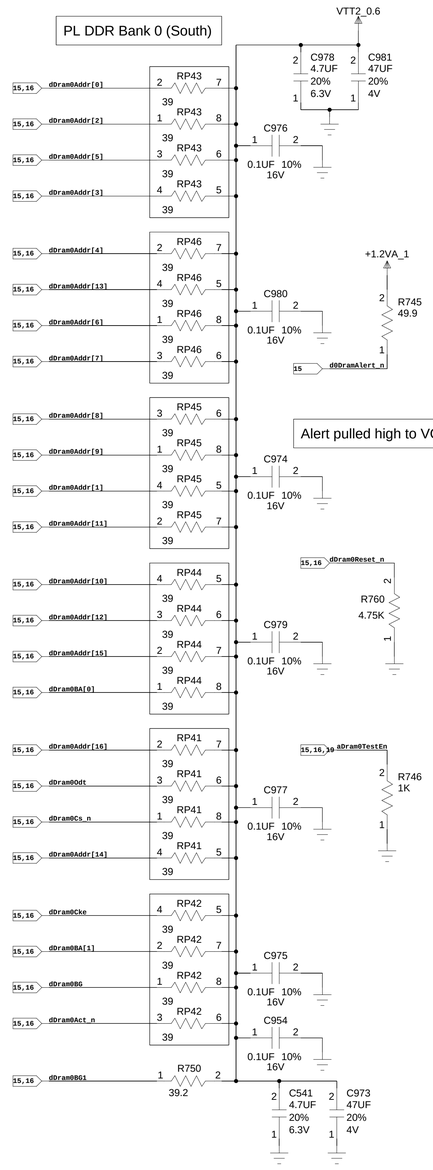
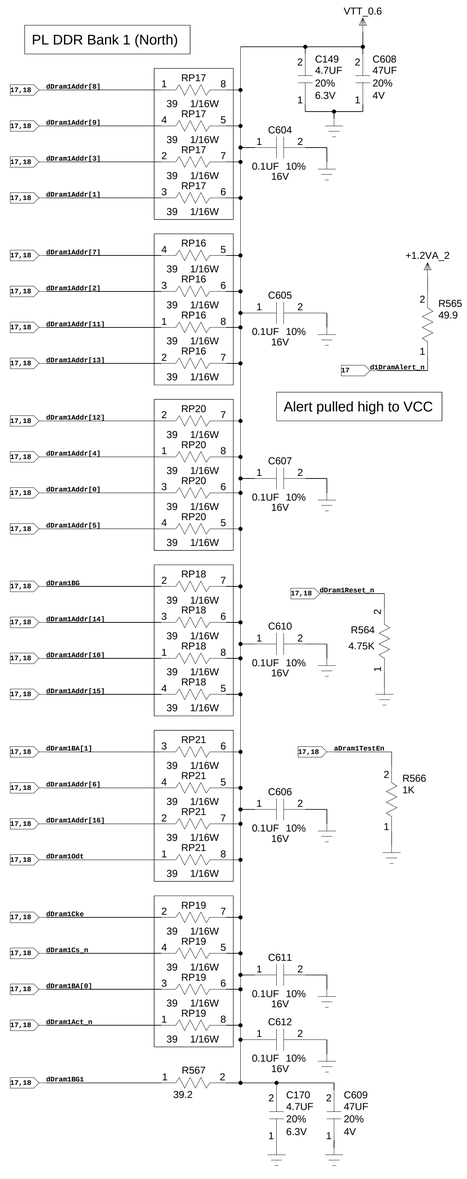
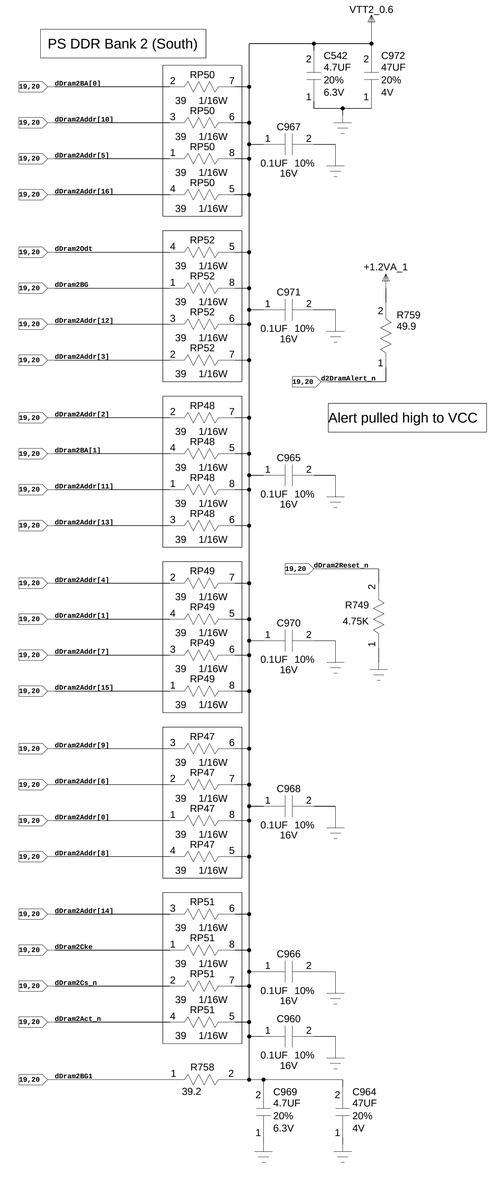


Figure 2-24: **Clock Fly-by Termination for DDR4 SDRAM**

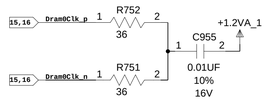
22. For address/command/control V_{TT} termination, every four termination resistors should be accompanied by one 0.1 µF capacitor, physically interleaving among resistors, as shown in Figure 2-13. Refer to the memory vendor's data sheet for specifications regarding noise limits on the address/command/control V_{TT} lines.

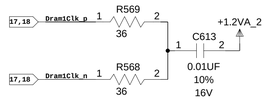


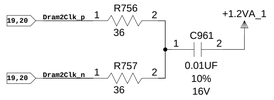




Clock terminates to VCCO







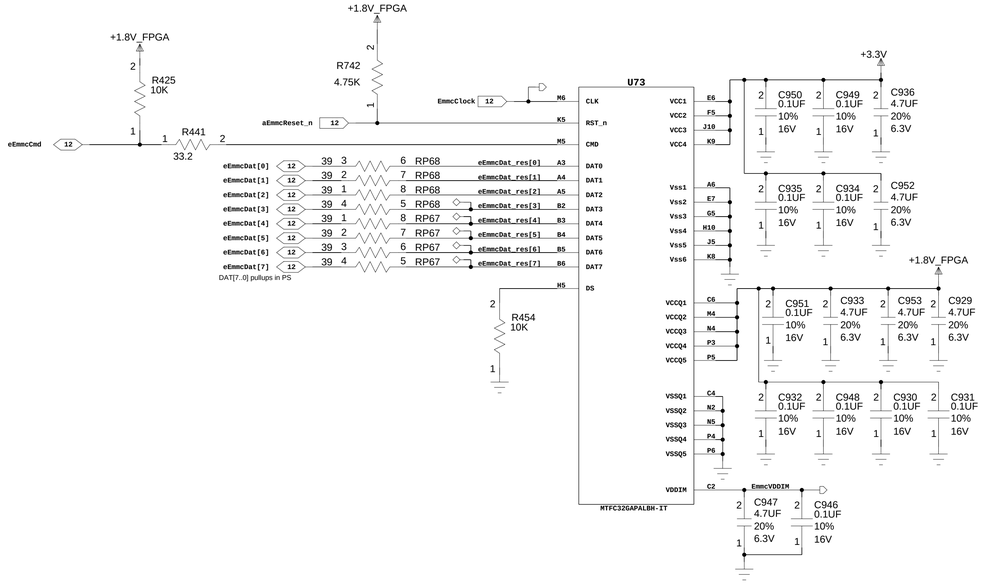
DDR4 Termination

USRP X410, BASECARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

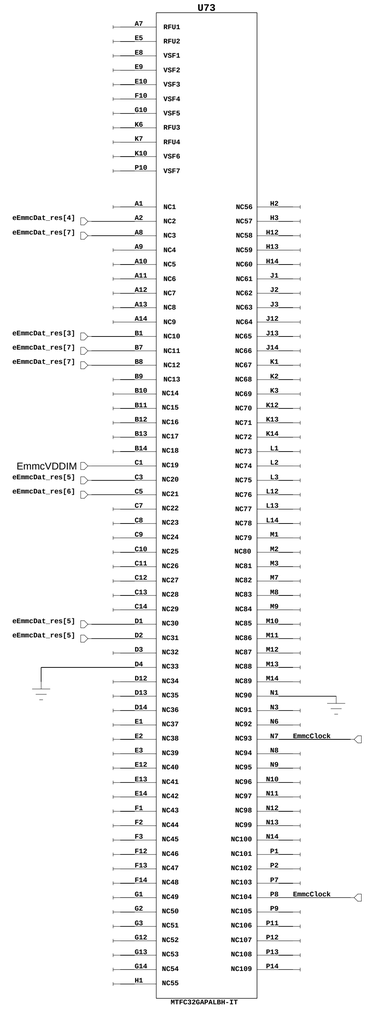
SCALE: NONE

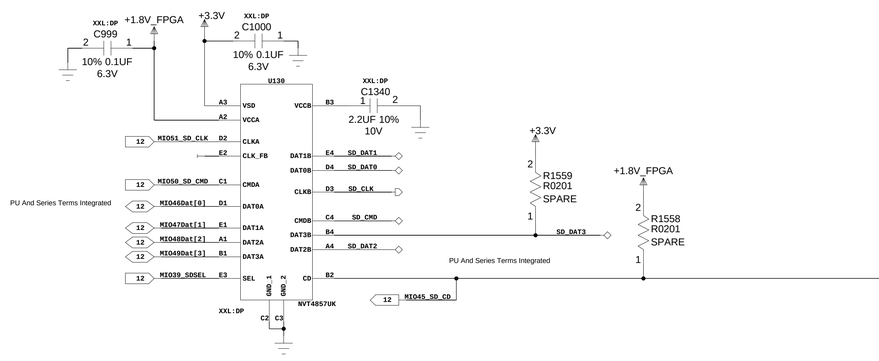
SHEET 21 OF 38

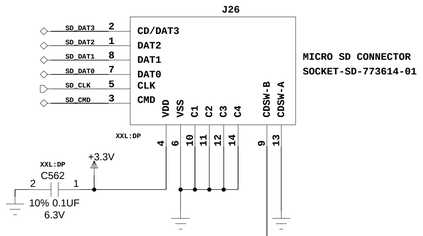


Layout: RFU pins should not be used as route-though pins.

NC pins are not connected in the package and can be used for route-through.





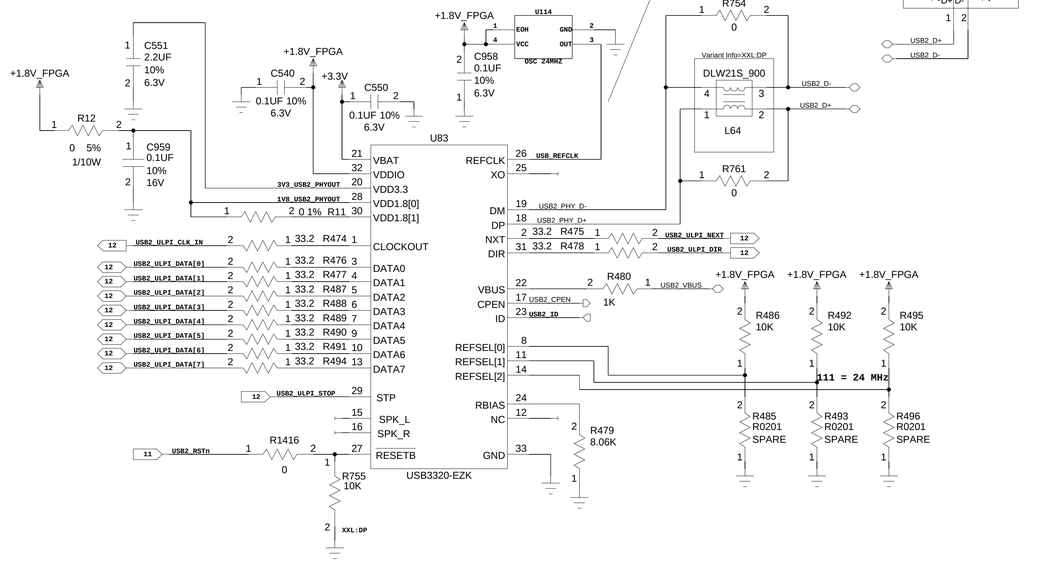


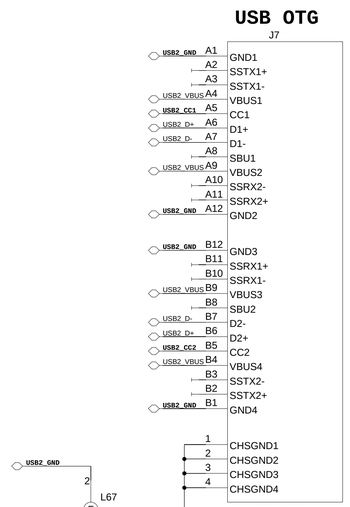
eMMC/uSD			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 22 OF 38	

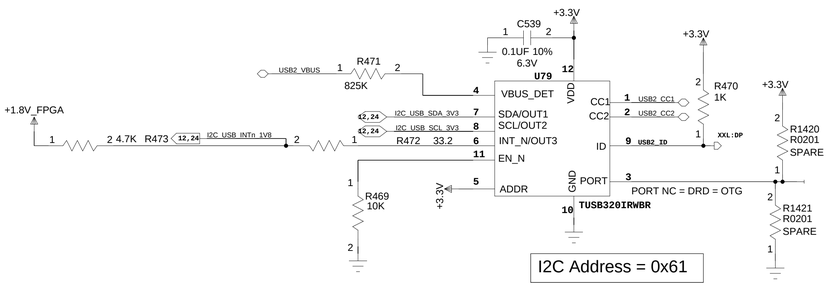
USB3340
remove R12 and R11
C959 1uF
C551 1UF

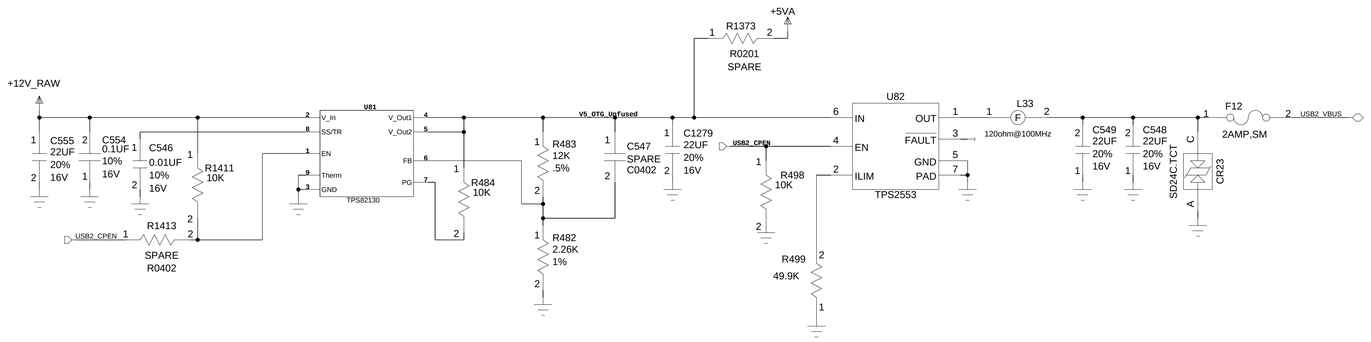
USB3320
add R12 and R11
C959 0.1uF
C551 2.2uF

LAYOUT: keep USB_REFCLK trace under 1.5" long

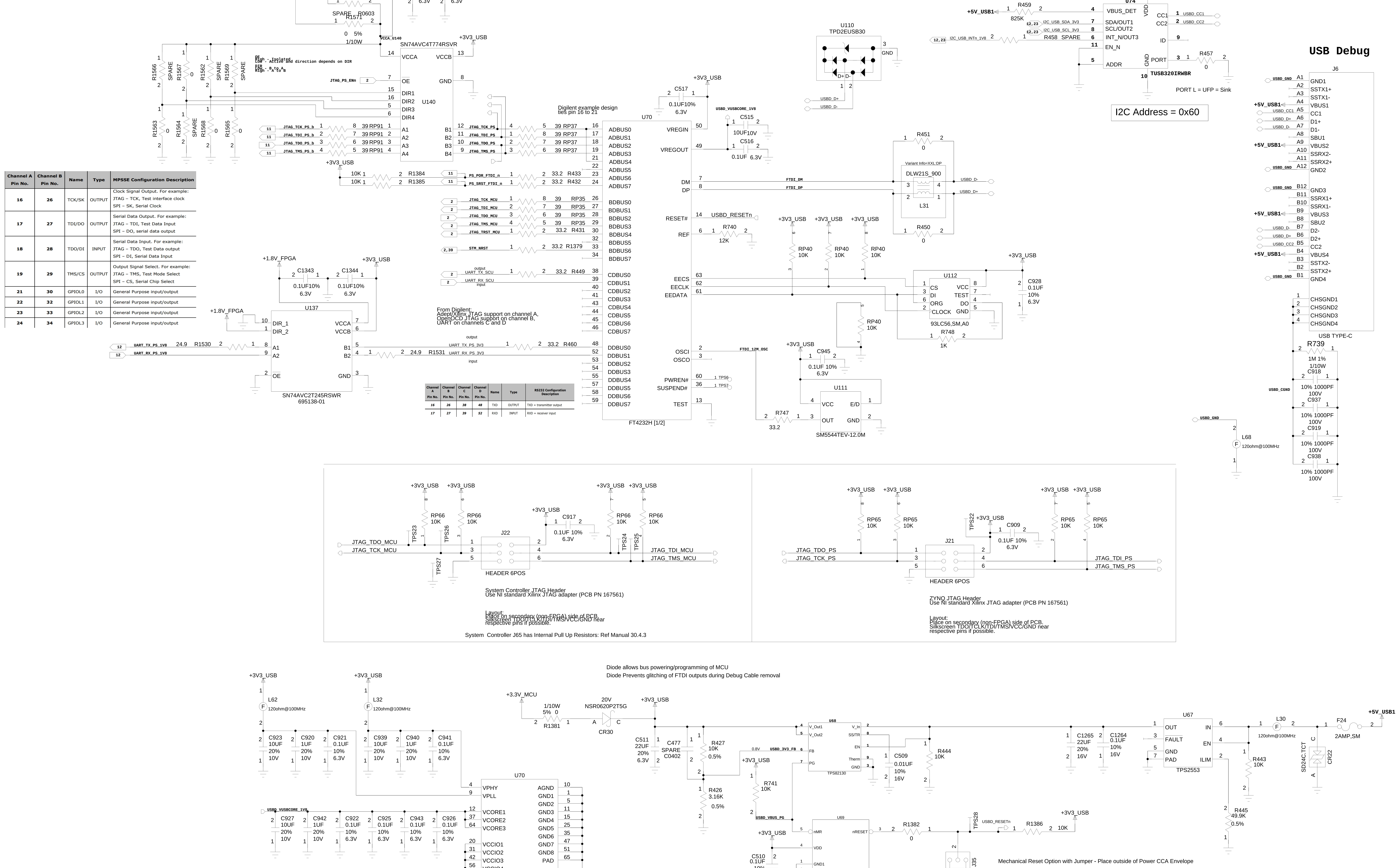








USB OTG			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 23 OF 38	

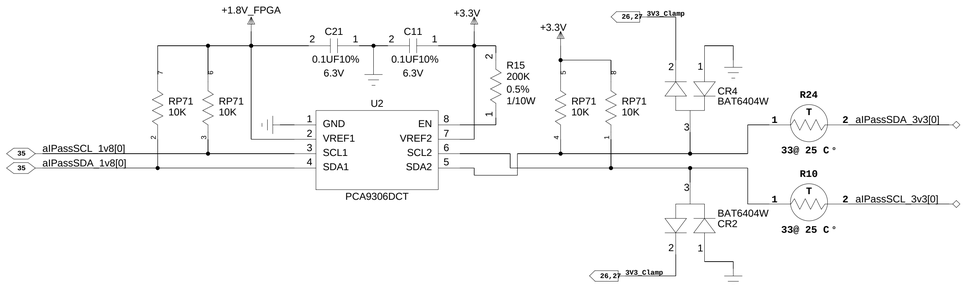


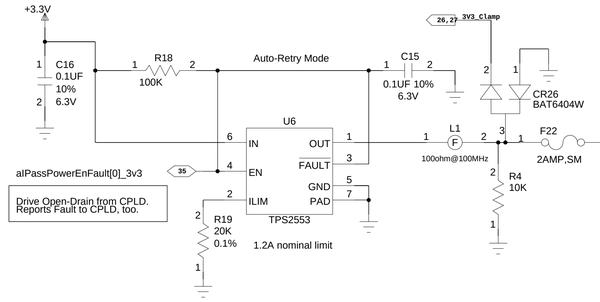
Channel A Pin No.	Channel B Pin No.	Name	Type	MPSSE Configuration Description
16	26	TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI – SK, Serial Clock
17	27	TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI – DO, serial data output
18	28	TDO/DI	INPUT	Serial Data Input. For example: JTAG – TDO, Test Data output SPI – DI, Serial Data Input
19	29	TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI – CS, Serial Chip Select
21	30	GPIOL0	I/O	General Purpose input/output
22	32	GPIOL1	I/O	General Purpose input/output
23	33	GPIOL2	I/O	General Purpose input/output
24	34	GPIOL3	I/O	General Purpose input/output

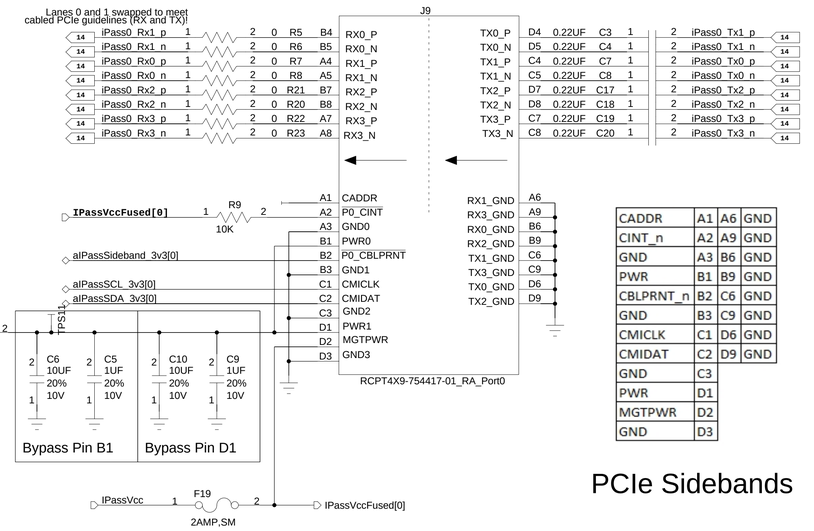
Channel A Pin No.	Channel B Pin No.	Channel C Pin No.	Channel D Pin No.	Name	Type	RS232 Configuration Description
16	26	38	48	TXD	OUTPUT	TXD = transmitter output
17	27	39	52	RXD	INPUT	RXD = receiver input

USB Debug			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 24 OF 38	

Connector 0

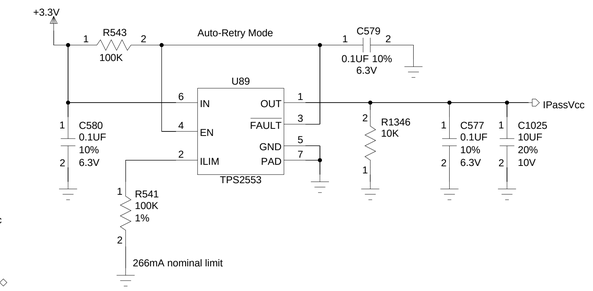


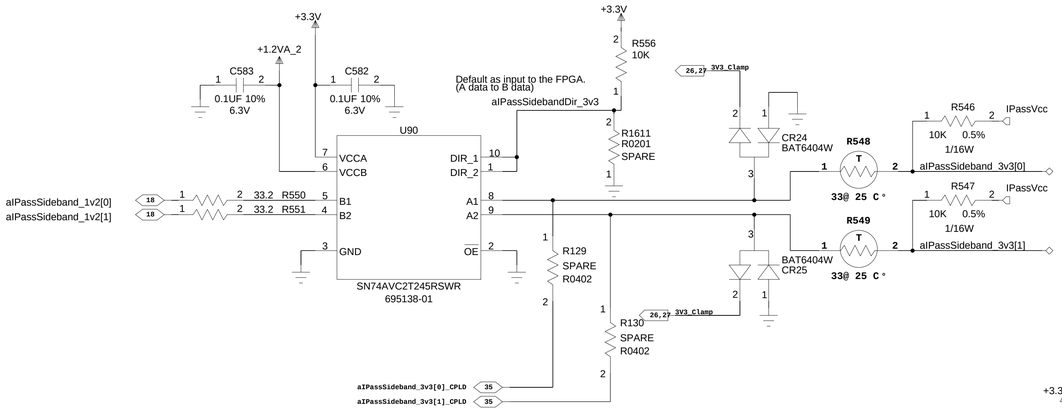




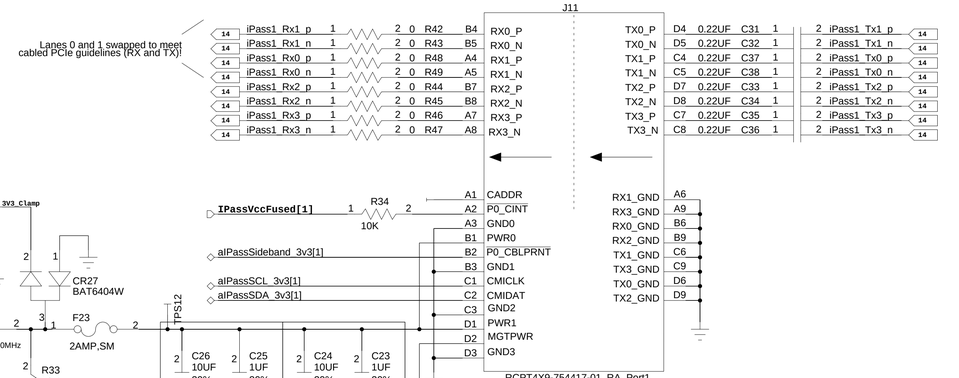
CADDR	A1	A6	GND
CINT_n	A2	A9	GND
GND	A3	B6	GND
PWR	B1	B9	GND
CBLPRNT_n	B2	C6	GND
GND	B3	C9	GND
CMICLK	C1	D6	GND
CMIDAT	C2	D9	GND
GND	C3		
PWR	D1		
MGTPWR	D2		
GND	D3		

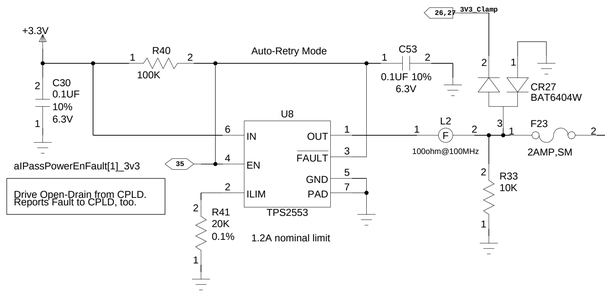
PCIe Sidebands

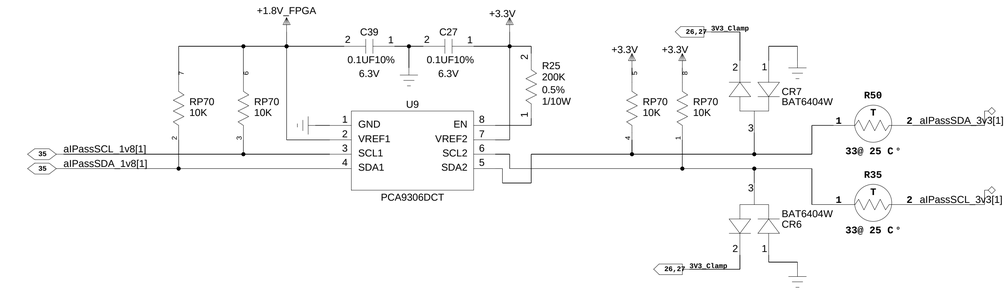


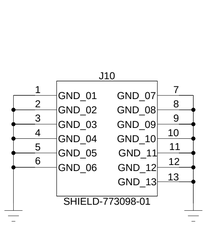


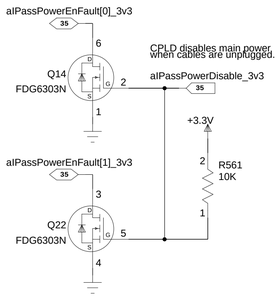
Connector 1









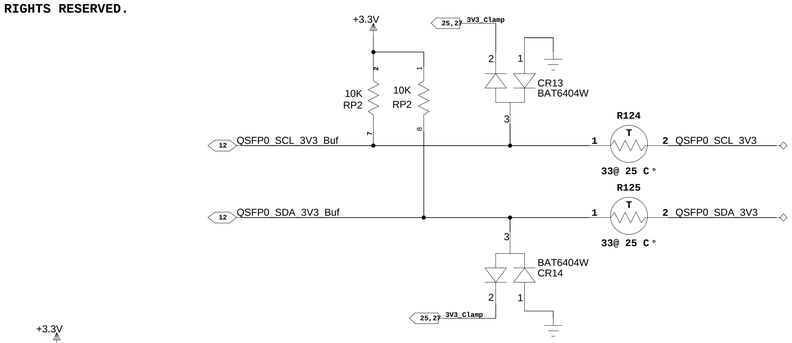


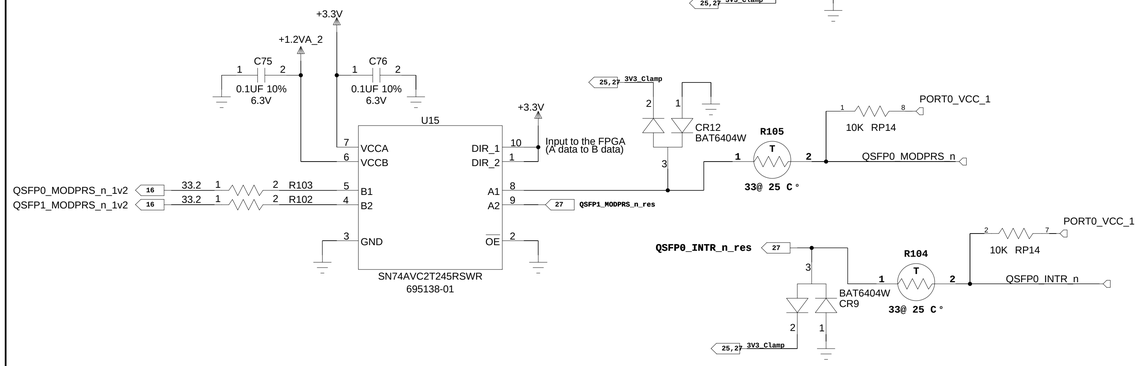
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6
SCALE: NONE		SHEET 25 OF 38	

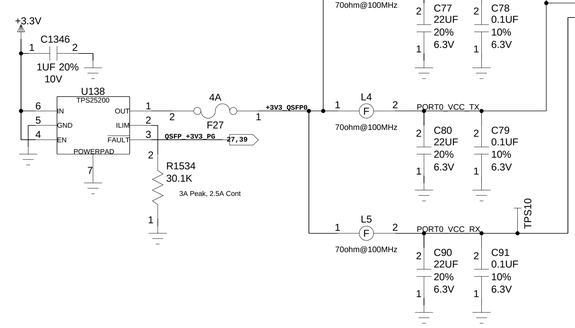
iPass+zHD Connectors

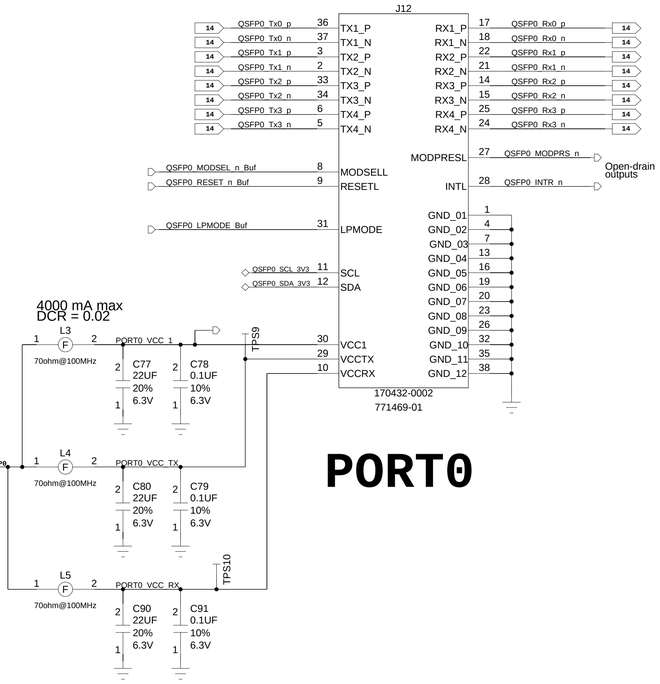
USRP X410, BASECARD

TX/RX on QSFPs are referenced to FPGA

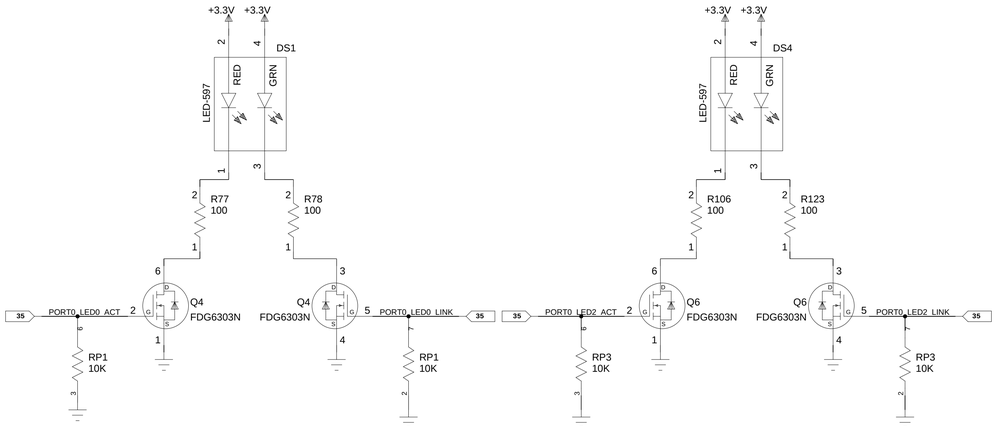


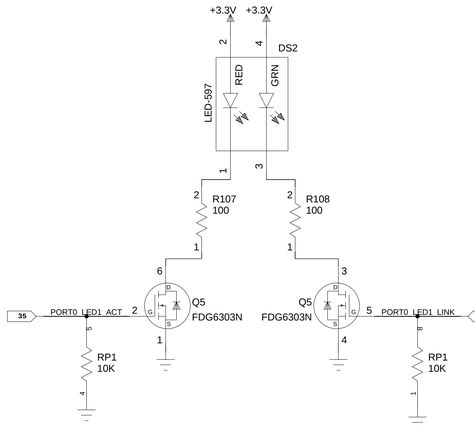


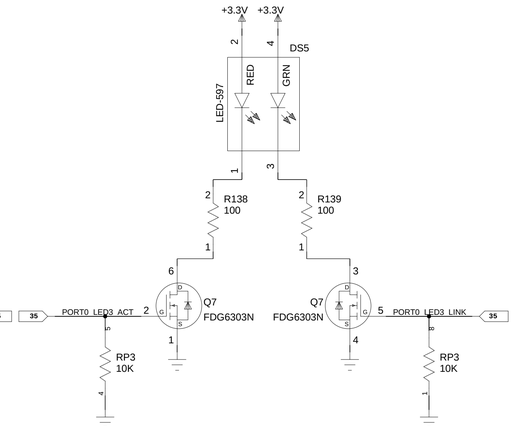


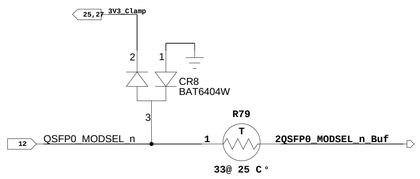


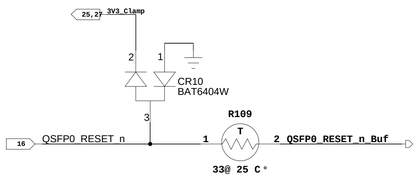
PORT0

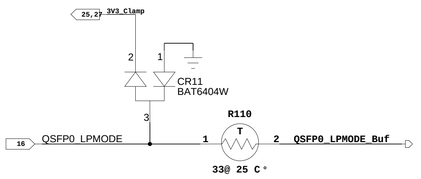


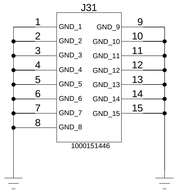












1x2 Cage, Quad LED

QSFP28 Port 0+Shield			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 26 OF 38	

TX/RX on QSFPs are referenced to FPGA

PORT1

4000 mA max
DCR = 0.02

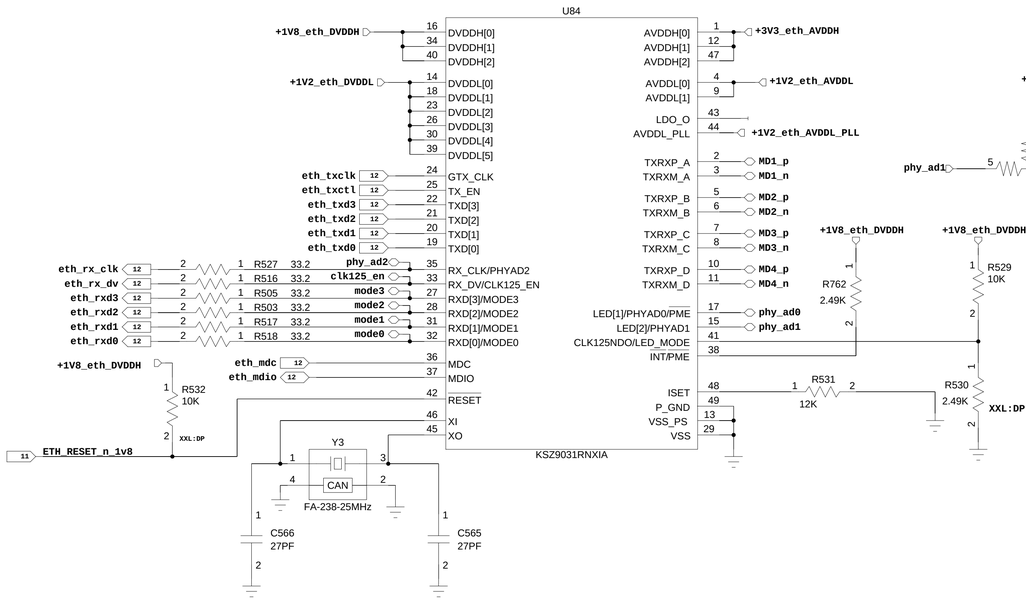
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

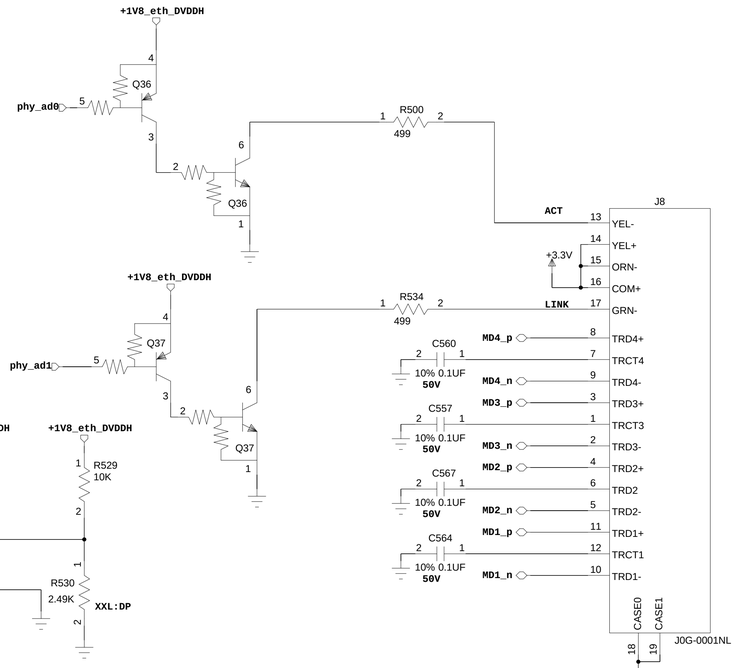
QSFP28 Port 1 + Protection

USRP X410, BASECARD

SCALE: NONE

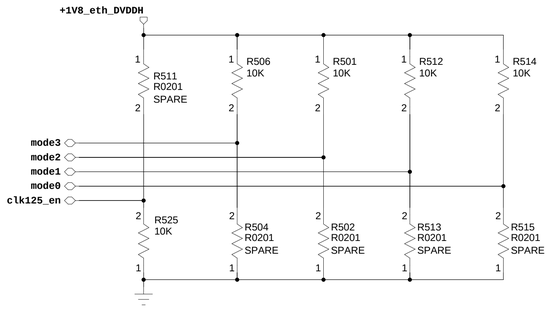
SHEET 27 OF 38



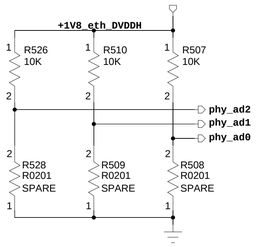


Ethernet Bootstrap Configuration

Mode/Clk Bootstraps
Mode: 15, clk disabled



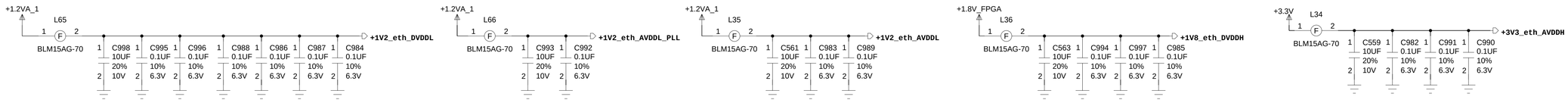
Address bootstraps
Currently configured for 0b111 (Phy address 7)



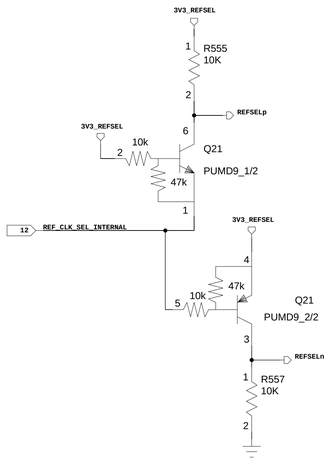
Layout: One cap should be placed near each shield connection

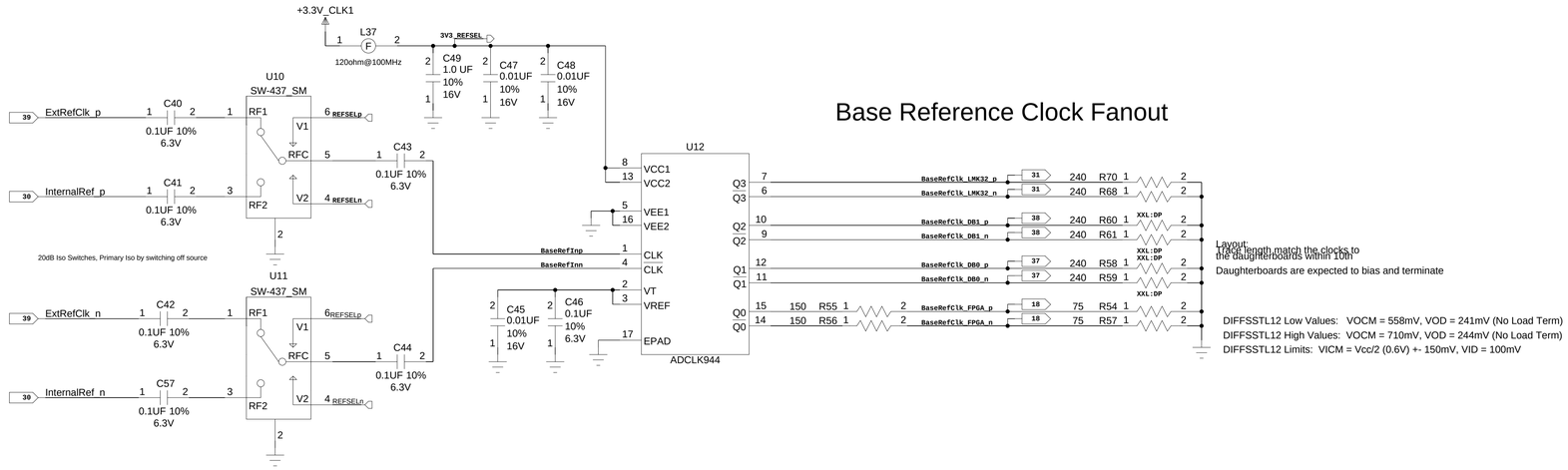
Ethernet Power Filtering

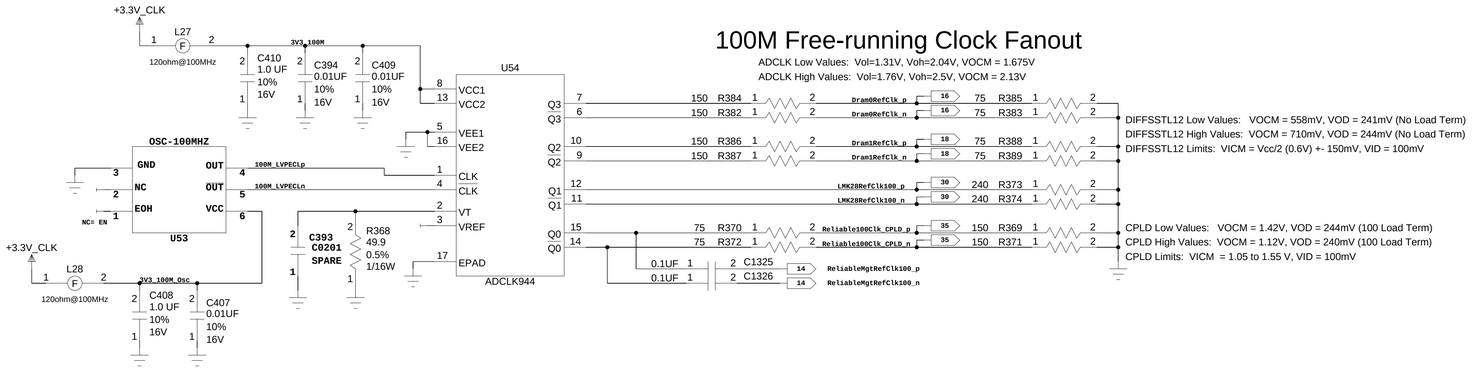
Layout has swapped from VA_2 to VA_1 due to placement



RJ45 Interface			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 28 OF 38	

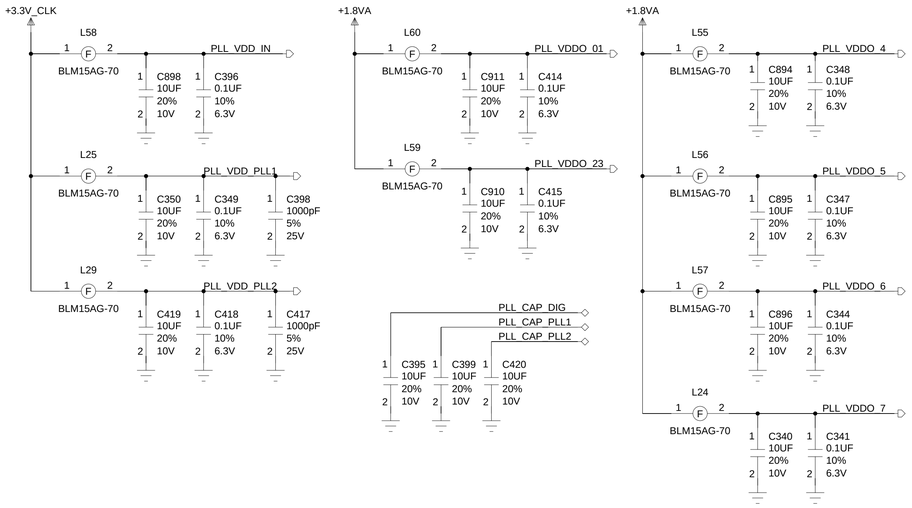




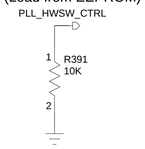


Reference Clocks			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 29 OF 38	

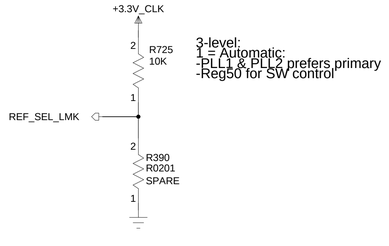
Place high freq. decoupling under QFN from plane via to thermal pad.

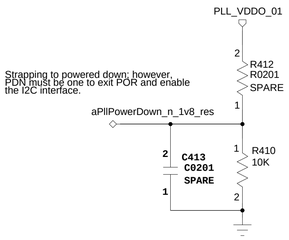


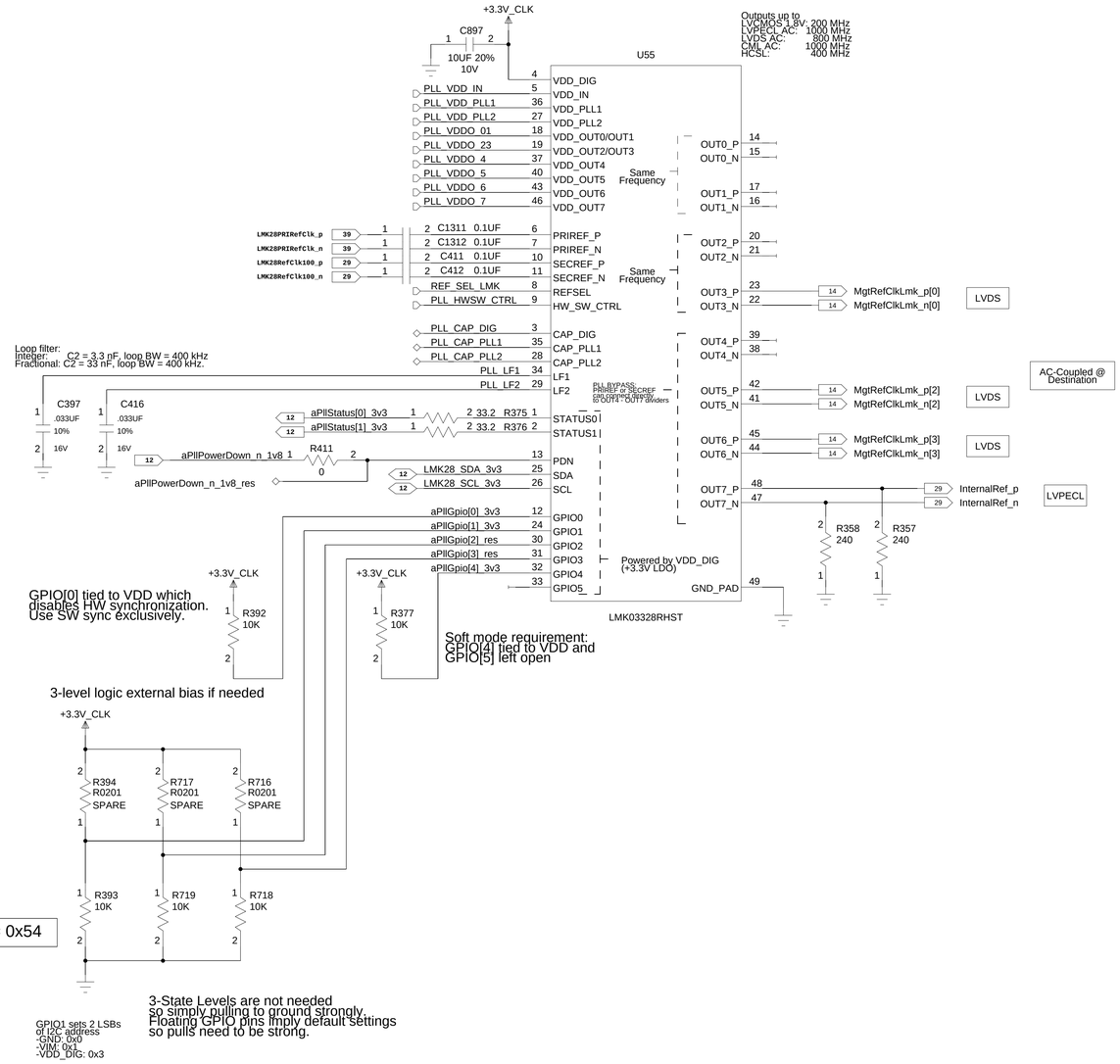
Soft mode
(Load from EEPROM)



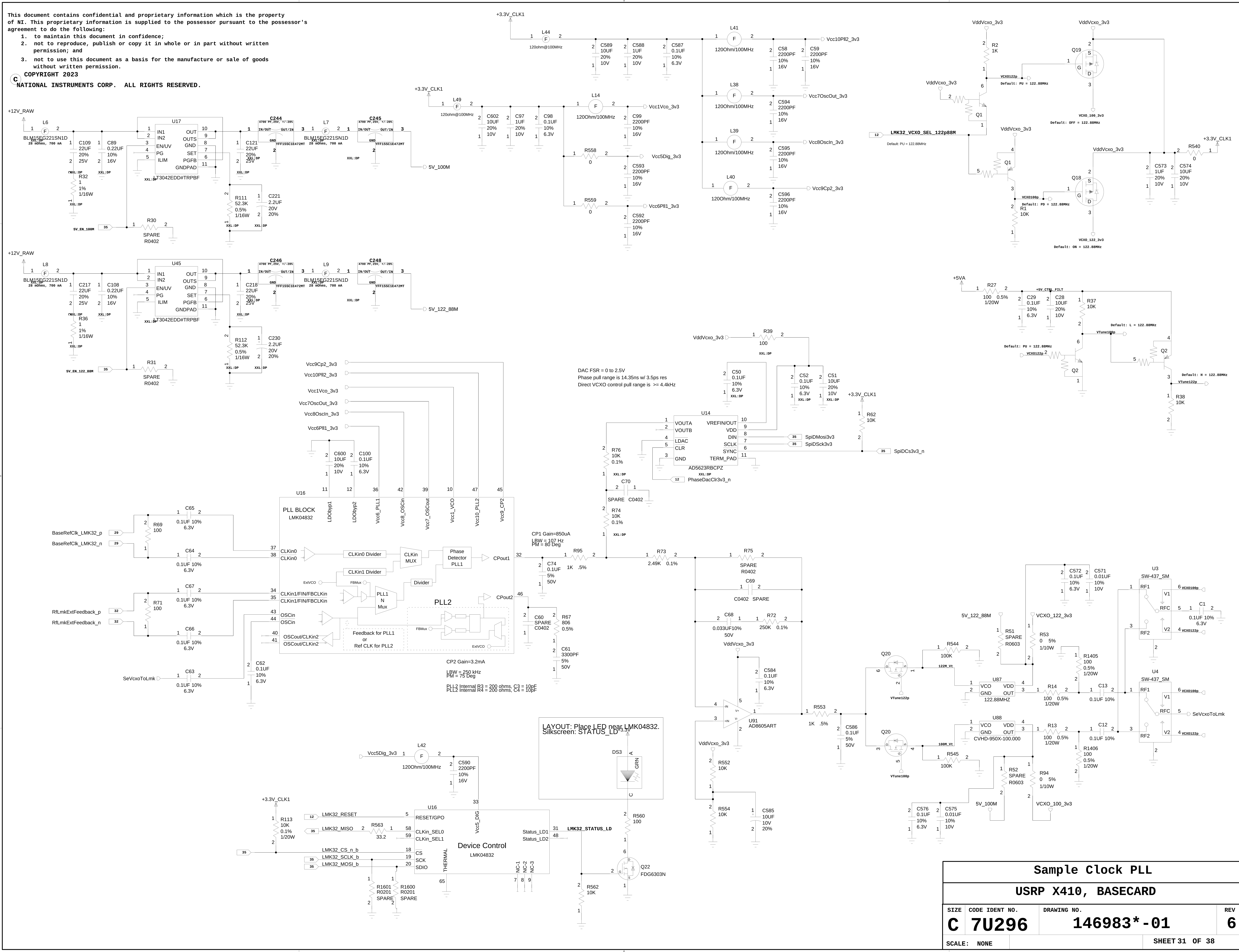
	LMK03328 Function		Chosen State for X400
LMK03328 Pin	Hard Mode (1)	Soft Mode (0)	
GPIO0	Selects 1 of 64 predefined settings from ROM	Active-low Output sync	pull-up: SW ctrl only
GPIO1		I2C dev. addr[1:0]	pull-down
GPIO2		Selects from 1 of 6 EEPROM pages or a default reg setting.	pull-downs, page 00 selected
GPIO3			
GPIO4		Active-low HW margin enable	pull-up, disable margin
GPIO5		HW margin level	floated
HW_SW_CTRL	Load registers from ROM or EEPROM		pull-down, SW ctrl
SCL	I2C clock		Ext. pull-up
SDA	I2C data		Ext. pull-up
PDN	Active-low power down		Ext. strong pull-down



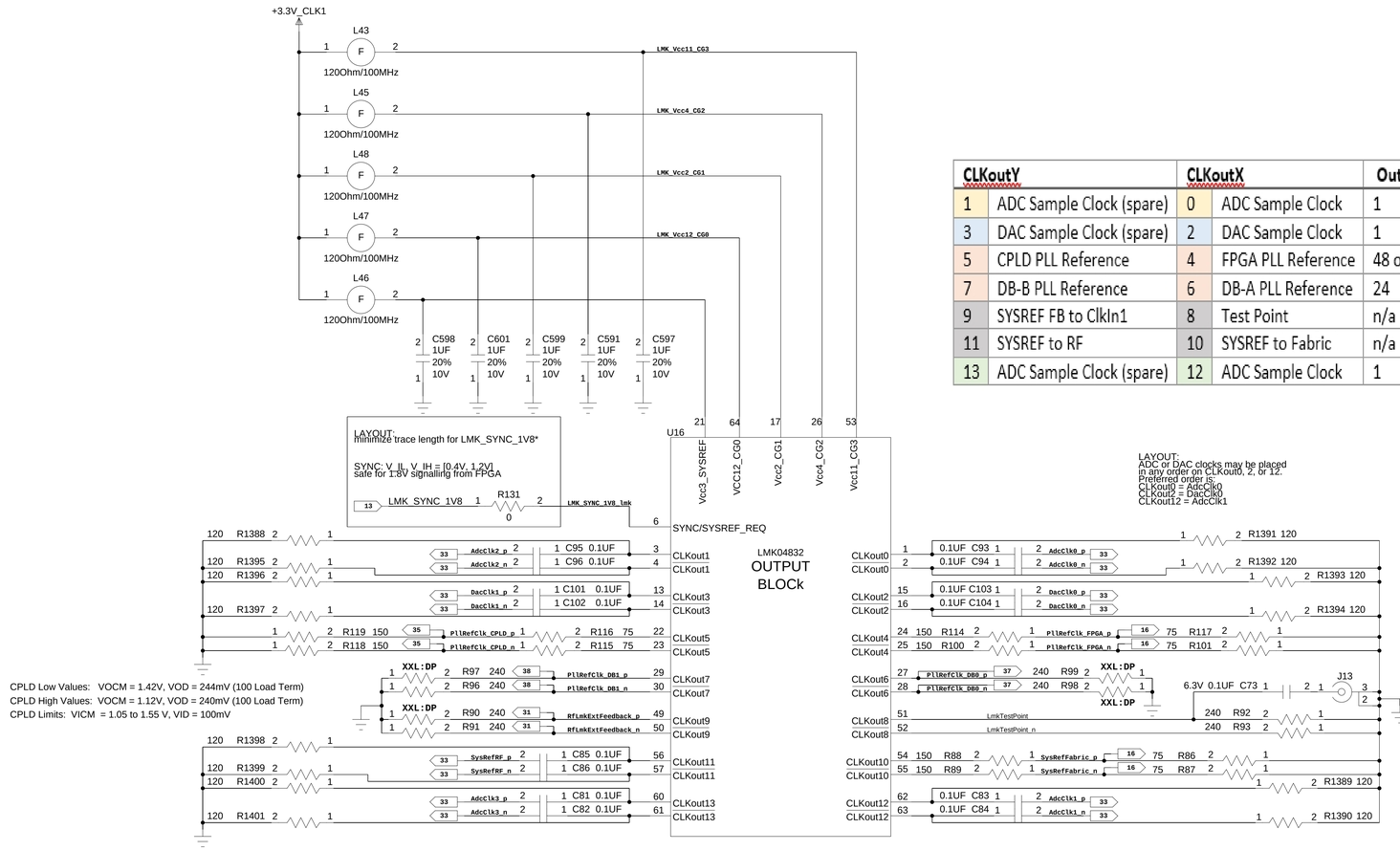




Reference Clock PLL				
USRP X410, BASECARD				
SIZE	CODE IDENT NO.	DRAWING NO.		REV
C	7U296	146983*-01		6
SCALE: NONE			SHEET 30 OF 38	



Sample Clock PLL			
USRP X410, BASECARD			
SIZE C	CODE IDENT NO. 7U296	DRAWING NO. 146983*-01	REV 6
SCALE: NONE		SHEET 31 OF 38	



CLKoutY		CLKoutX		Output Divider
1	ADC Sample Clock (spare)	0	ADC Sample Clock	1
3	DAC Sample Clock (spare)	2	DAC Sample Clock	1
5	CPLD PLL Reference	4	FPGA PLL Reference	48 or 60
7	DB-B PLL Reference	6	DB-A PLL Reference	24
9	SYSREF FB to ClkIn1	8	Test Point	n/a
11	SYSREF to RF	10	SYSREF to Fabric	n/a
13	ADC Sample Clock (spare)	12	ADC Sample Clock	1

Sample Clock PLL Outputs

USRP X410, BASECARD

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

SCALE: NONE

SHEET 32 OF 38

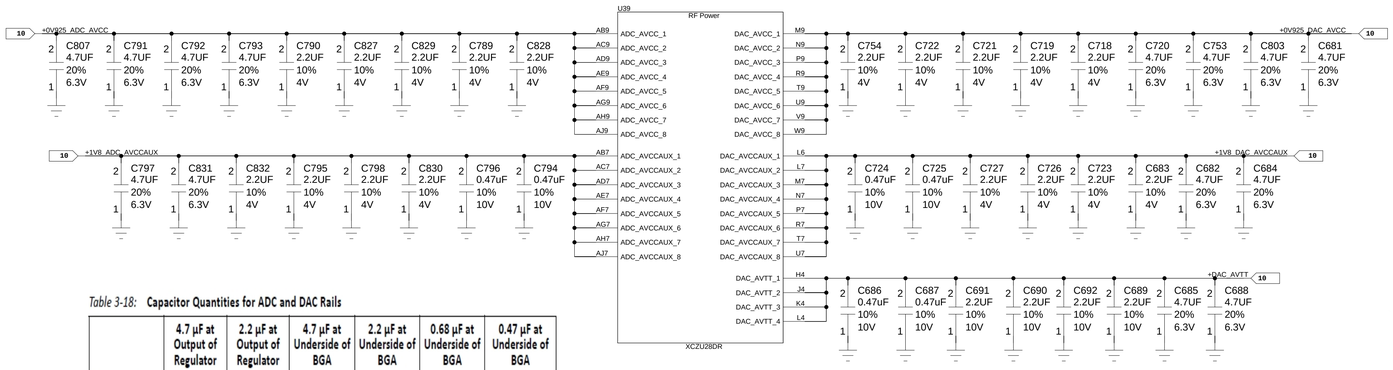


Table 3-18: **Capacitor Quantities for ADC and DAC Rails**

	4.7 µF at Output of Regulator	2.2 µF at Output of Regulator	4.7 µF at Underside of BGA	2.2 µF at Underside of BGA	0.68 µF at Underside of BGA	0.47 µF at Underside of BGA
ADC_AVCC	2	2	2	3	0	0
ADC_AVCCAUX	2	2	0	2	1	1
DAC_AVCC	2	2	2	3	0	0
DAC_AVCCAUX	2	2	0	2	1	1
DAC_AVTT	2	2	0	2	1	1

Table 3-14: **ADC and DAC Voltage Supply Specifications**

Supply	Nominal Voltage (V)	Tolerance (%)[1]	Maximum Current (A)	Frequency Range (MHz)	Maximum Supply Ripple (mVpp)[2]
ADC_AVCC	0.925	±3	XPE*	0.1-15	0.25
ADC_AVCCAUX	1.8	±3	XPE*	0.1-15	11.03
DAC_AVCC	0.925	±3	XPE*	0.1-15	0.40
DAC_AVCCAUX	1.8	±3	XPE*	0.1-15	2.00
DAC_AVTT	2.5/3.0[3]	±3	XPE*	0.1-15	8.94
VCCINT_AMS	0.85/0.90	±3	XPE*	0.1-15	20.00

Notes:
1. The tolerance percentage is for the switching regulator that feeds the LDO.
2. Output of the LDO.
3. DAC_AVTT should be set to 2.5V if used in 20 mA mode, and 3.0V if used in 32 mA mode.

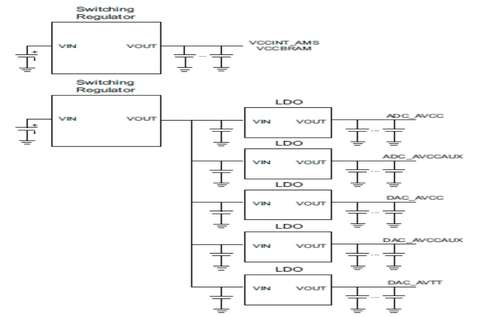
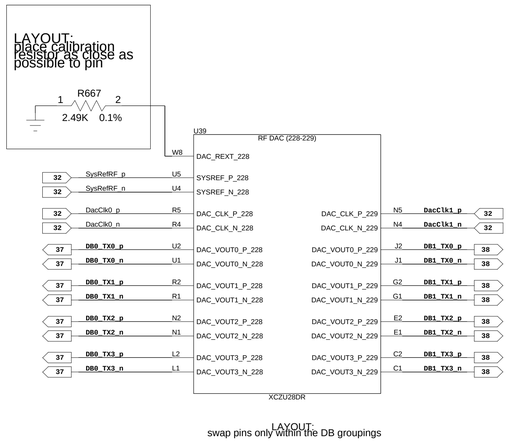
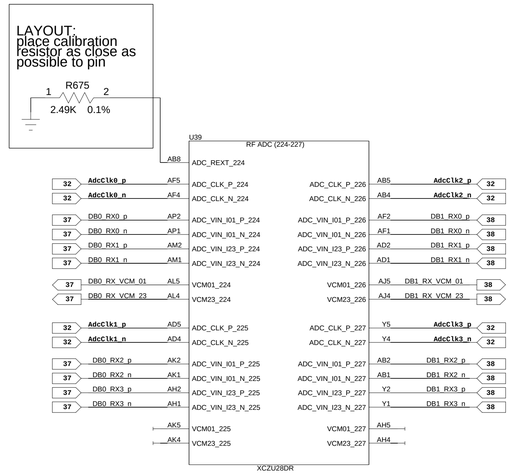


Figure 3-14: **Power Regulation for Analog Supplies**

RF Bank Mapping		
	RF Bank	Destination
ADC	Bank 224	DB0, Ch. 0-1
	Bank 225	DB1, Ch. 0-1
	Bank 226	DB0, Ch. 2-3
	Bank 227	DB1, Ch. 2-3
DAC	Bank 228	DB0, Ch. 0-3
	Bank 229	DB1, Ch. 0-3



LAYOUT:
swap pins only within the DB groupings



LAYOUT:
swap pins only within the DB groupings

RF Interface and Power

USRP X410, BASECARD

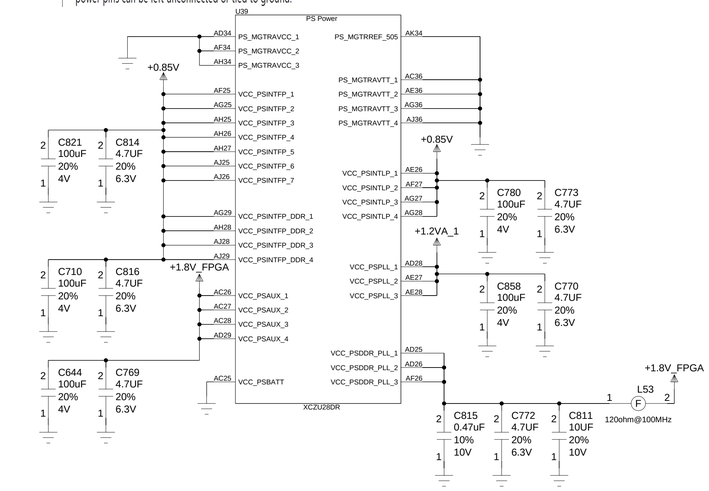
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6

SCALE: NONE

SHEET 33 OF 38

PS_MGTRAVCC	• If all of the PS-GTR transceivers in the Quad are not used, the associated power pins can be left unconnected or tied to ground.

PS_MGTRREF	• Connect to a 500Ω 0.5% resistor to this pin with the other terminal of the resistor connected to ground. • Can be left unconnected or tied to ground if the transceivers will not be used.



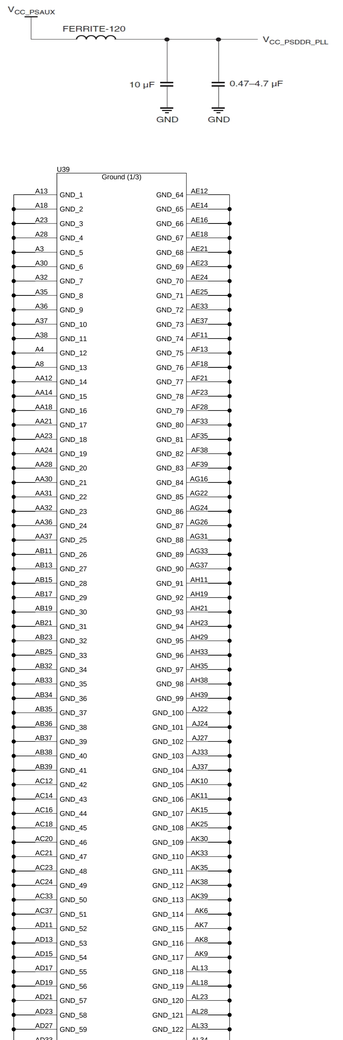


Table 3-3: **Decoupling Capacitor Quantities for $V_{CCSDFEC}$, plus additional capacitors for V_{CCBRAM}/V_{CCINT_IO}**

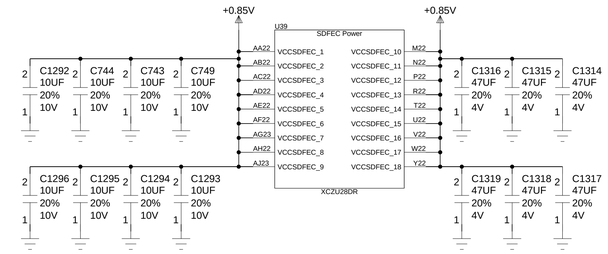
$V_{CCSDFEC}$			V_{CCBRAM}/V_{CCINT_IO}
10 µF 0805	4.7 µF 0603	1.0 µF 0402	1.0 µF 0402
3	6	8	4

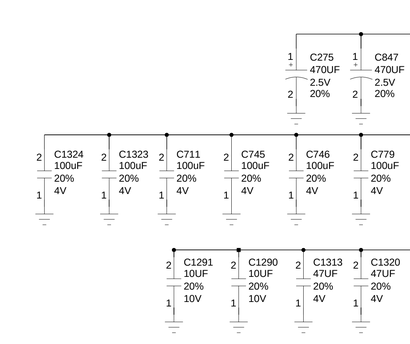
Notes:
1. This table only applies for when $V_{CCSDFEC}$ is utilized.
2. V_{CCBRAM}/V_{CCINT_IO} capacitors are in addition to those in Table 3-1 and Table 3-2.
3. See Table 3-4 for connection rules for these capacitors.

Table 3-4 lists the placement rules for the capacitors in Table 3-3. Refer to Figure 3-1 for visual reference.

Table 3-4: **Placement Rules for Additional $V_{CCSDFEC}/V_{CCBRAM}/V_{CCINT\_IO}$ Decoupling Capacitors**

Capacitor	Rule
10 µF 0805	All three next to FPGA footprint near $V_{CCSDFEC}$ and V_{CCBRAM}/V_{CCINT_IO} merge point.
4.7 µF 0603	All six next to FPGA footprint near $V_{CCSDFEC}$ and V_{CCBRAM}/V_{CCINT_IO} merge point.
1.0 µF 0402	• Eight connected to $V_{CCSDFEC}$ plane under FPGA shadow. • Two connected under V_{CCBRAM} ball area between via plating holes. • Two connected under V_{CCINT_IO} ball area between via plating holes.





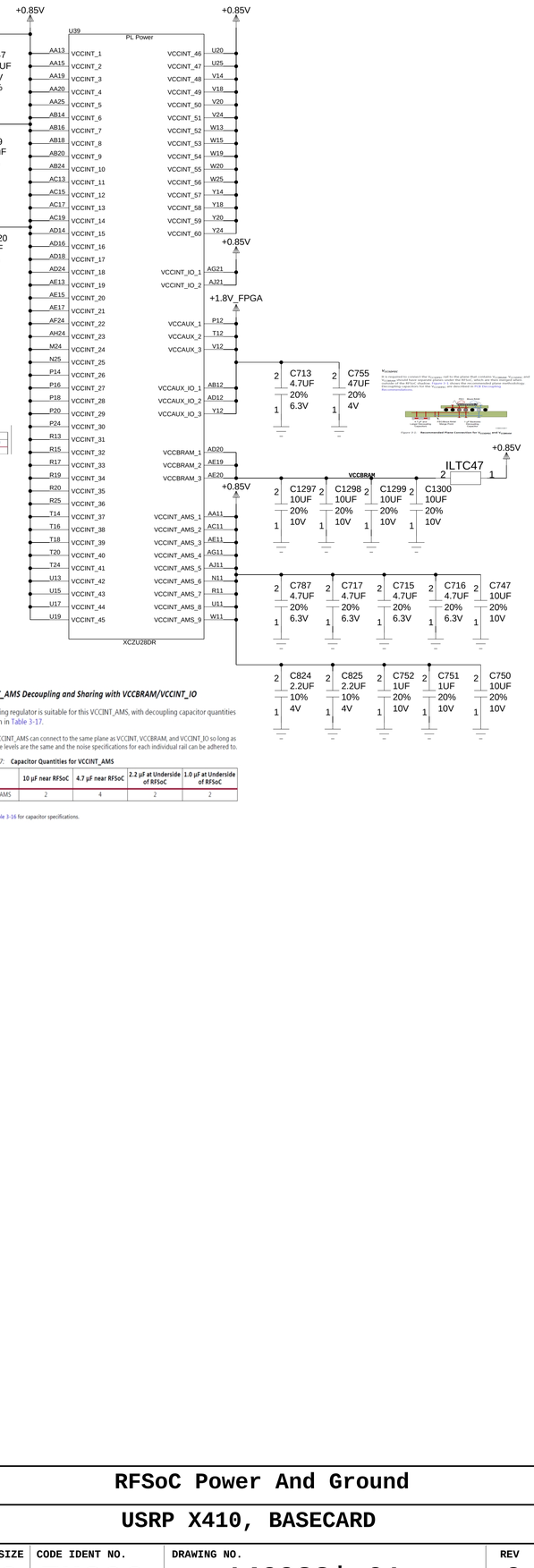


Table 3-1: **Programmable Logic Rail Decoupling Guidelines for Non-L Devices**

RFSoC	$V_{CCINT}/V_{CCBRAM}/V_{CCINT\_IO}$			V_{CCAUX}/V_{CCAUX_IO}		V_{CCO}	
	680 µF	100 µF	4.7 µF	47 µF	4.7 µF	47 µF	4.7 µF
XCZU28DR-FFVG1517	2	4	6	1	2	1	2

VCCINT_AMS Decoupling and Sharing with VCCBRAM/VCCINT_IO

A switching regulator is suitable for this VCCINT_AMS, with decoupling capacitor quantities as shown in Table 3-17.

Note: VCCINT_AMS can connect to the same plane as VCCINT, VCCBRAM, and VCCINT_IO so long as all voltage levels are the same and the noise specifications for each individual rail can be adhered to.

Table 3-17: **Capacitor Quantities for VCCINT_AMS**

	10 µF near RFSoC	4.7 µF near RFSoC	2.2 µF at Underside of RFSoC	1.0 µF at Underside of RFSoC
VCCINT_AMS	2	4	2	2

Notes:
1. See Table 3-16 for capacitor specifications.

Table 1-10: **Zynq UltraScale+ MPSoC PS Decoupling Capacitor Recommendations**

$V_{CC\_PSINTLP}$		$V_{CC\_PSINTFP}$		V_{CC_PSAUX}		V_{CC_PSPLL}		PS_ MGTRAVCC	PS_ MGTRAVTT	$V_{CC\_PSINTFP\_DDR}$		V_{CCO_PSIO} [3] (Each)		V_{CC_PSBATT}		V_{CCO_PSDDR}		
100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	4.7 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	100 µF	4.7 µF	0.47 µF
1	1	1	1	1	1	1	1	See note 1	See note 1	1	1	1	1	1	1	1	2	4

Notes:
1. For PS MGT supply decoupling, see PS-GTR Transceiver Interfaces, page 179.
2. Add two 0.47 µF capacitors to each PS voltage rail if using SBVA484 devices.
3. V_{CCO_PSIO} banks that share the same rail can utilize one set of decoupling capacitors (1 x 100 µF, 1 x 4.7 µF) for up to four connected VCCO_PSIO banks.

Consolidation is page 37 of UG583:

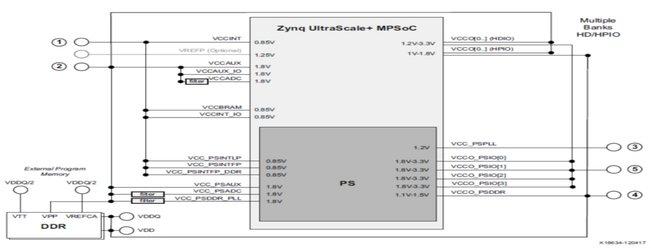
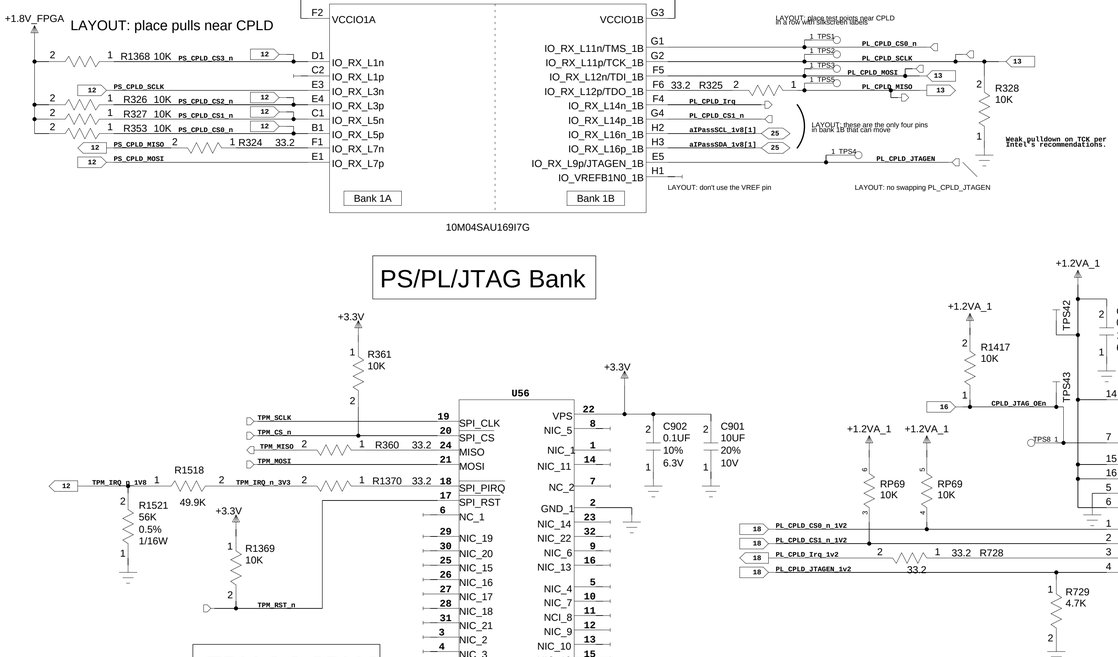


Figure 1-6: **Always On: Cost-Optimized with Only Five Power Regulators (CG or EG Devices)**

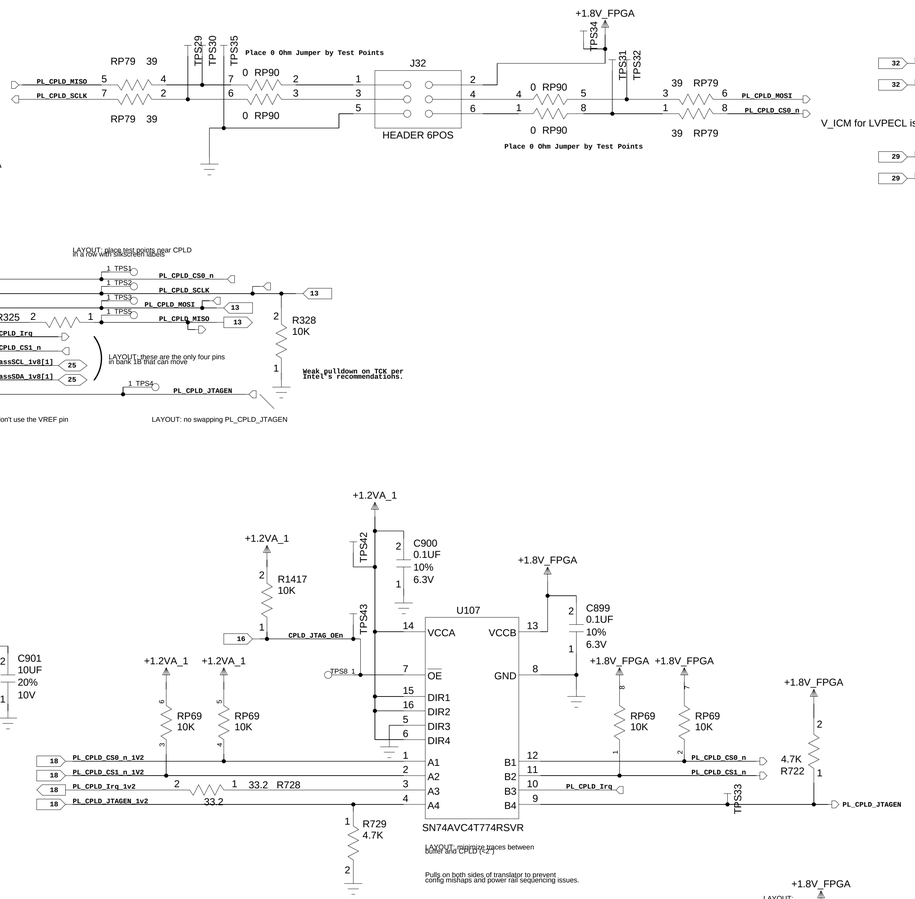
RFSOC POWER AND GROUND			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 34 OF 38	

PS/PL/JTAG Bank

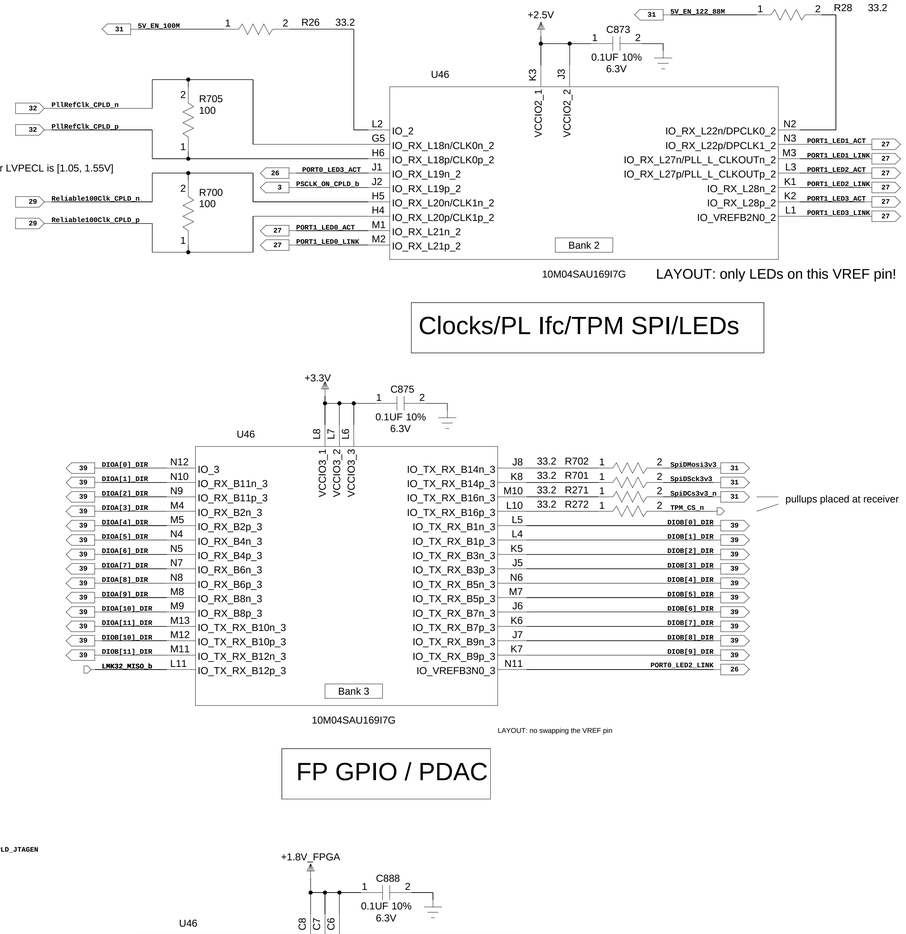


TPM 2.0 SPI IC

Level Translator

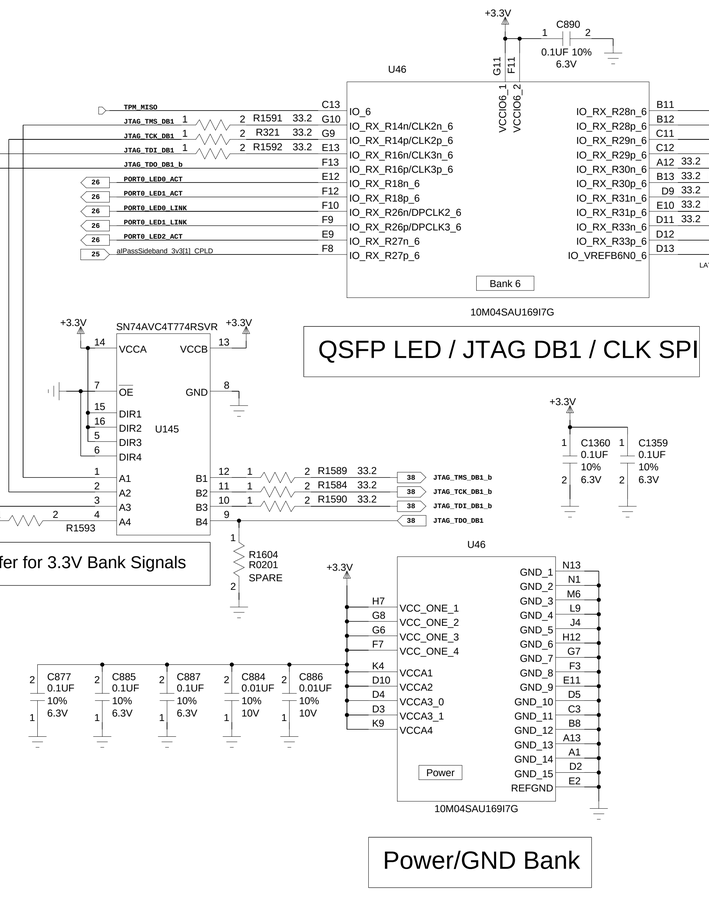


Clocks/PL Ifc/TPM SPI/LEDs



FP GPIO / PDAC

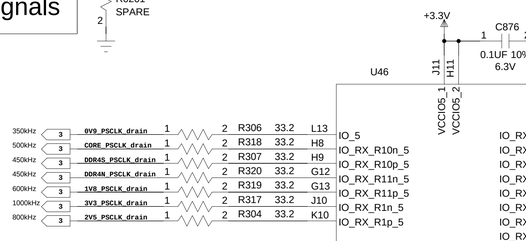
QSFP LED / JTAG DB1 / CLK SPI



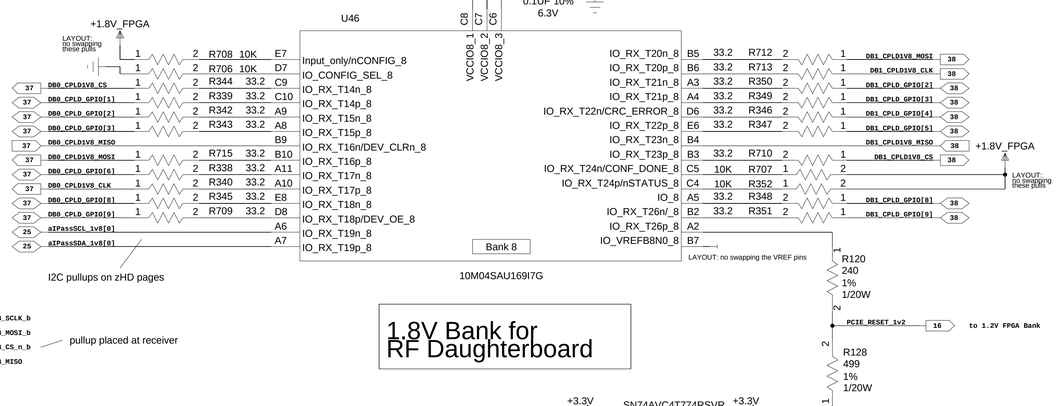
Buffer for 3.3V Bank Signals

Power/GND Bank

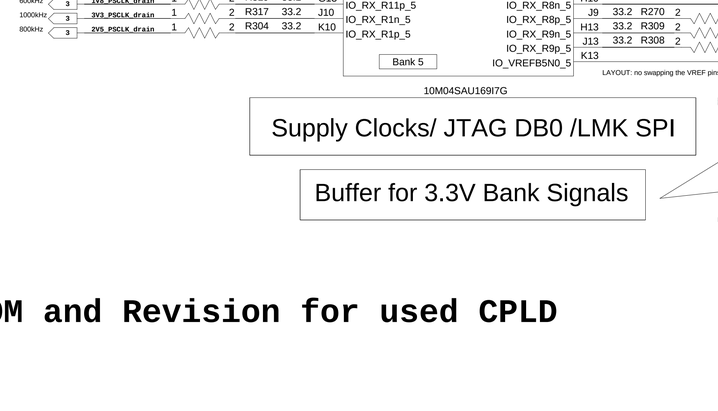
Buffer for 3.3V Bank Signals



1.8V Bank for RF Daughterboard



Supply Clocks/ JTAG DB0 /LMK SPI

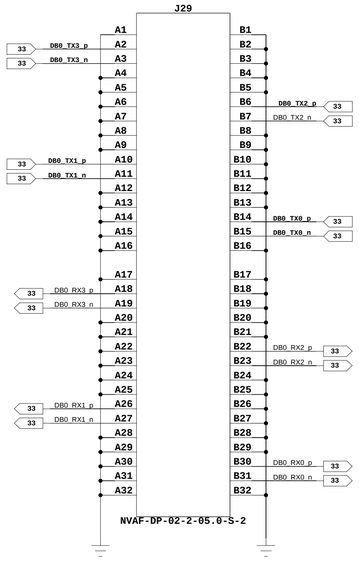


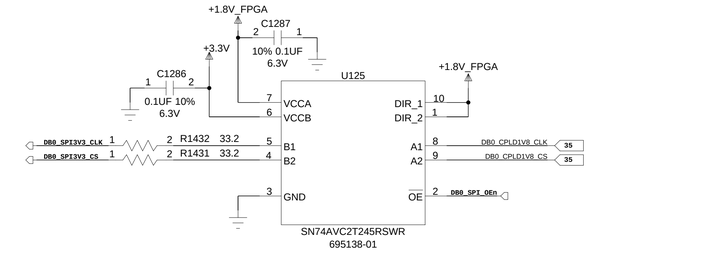
Buffer for 3.3V Bank Signals

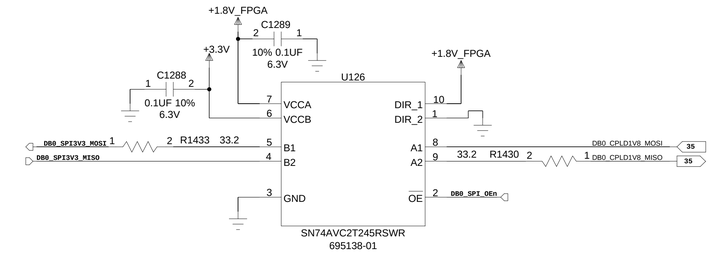
CAUTION: Check BOM and Revision for used CPLD

Control CPLD			
USRP X410, BASECARD			
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	7U296	146983*-01	6
SCALE: NONE		SHEET 35 OF 38	

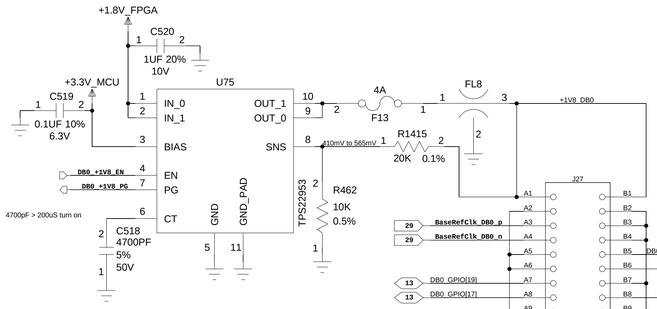
RF Board-Board

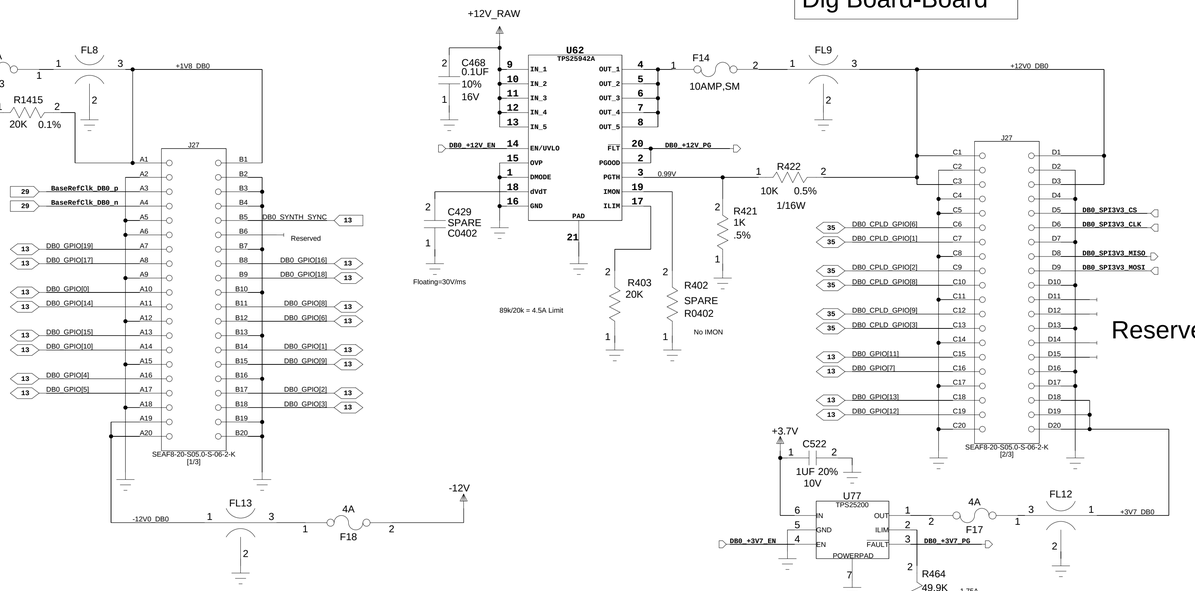


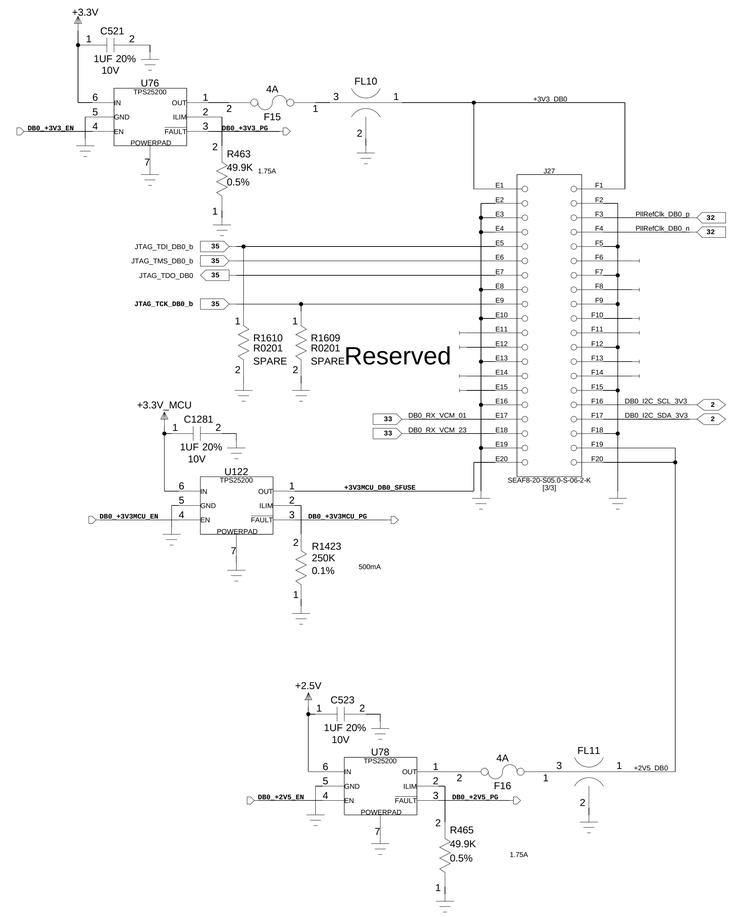




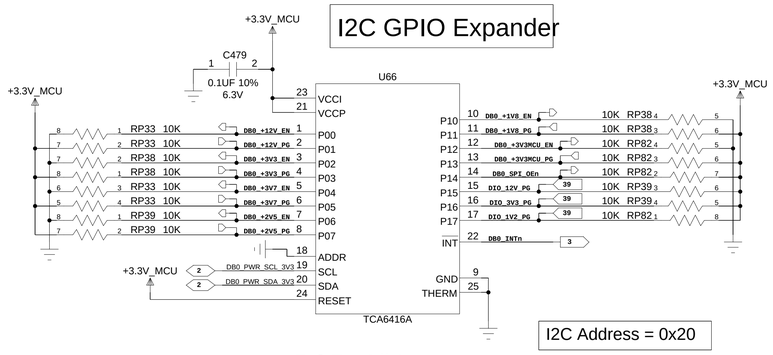
Dig Board-Board







I2C GPIO Expander

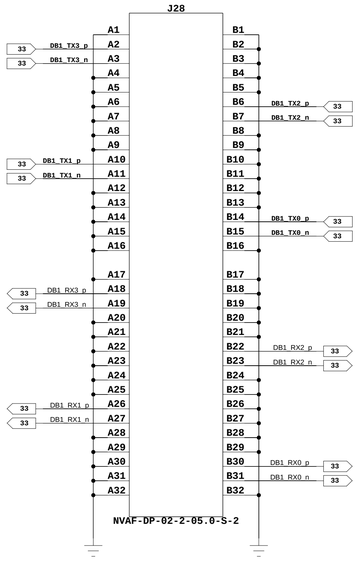


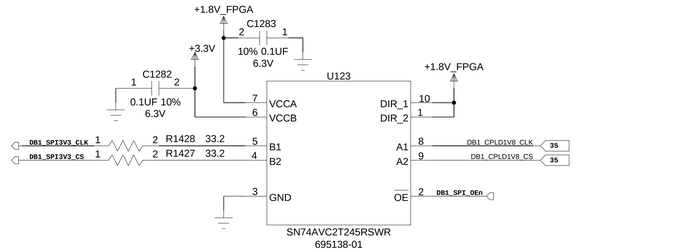
I2C Address = 0x20

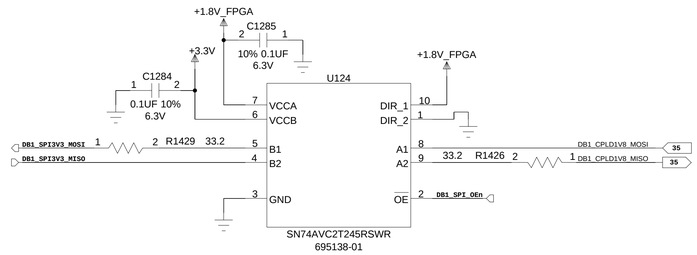
POR: All Inputs
RESET Active Low!

Daughtercard 0 Interface			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 36 OF 38	

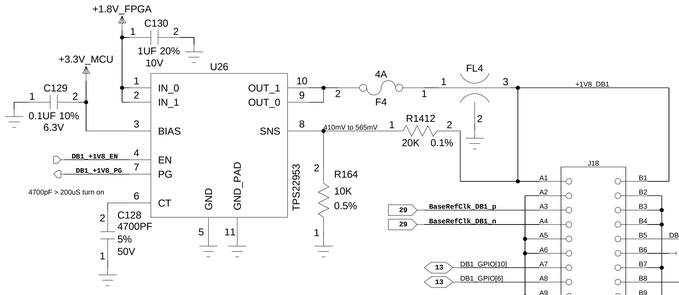
RF Board-Board

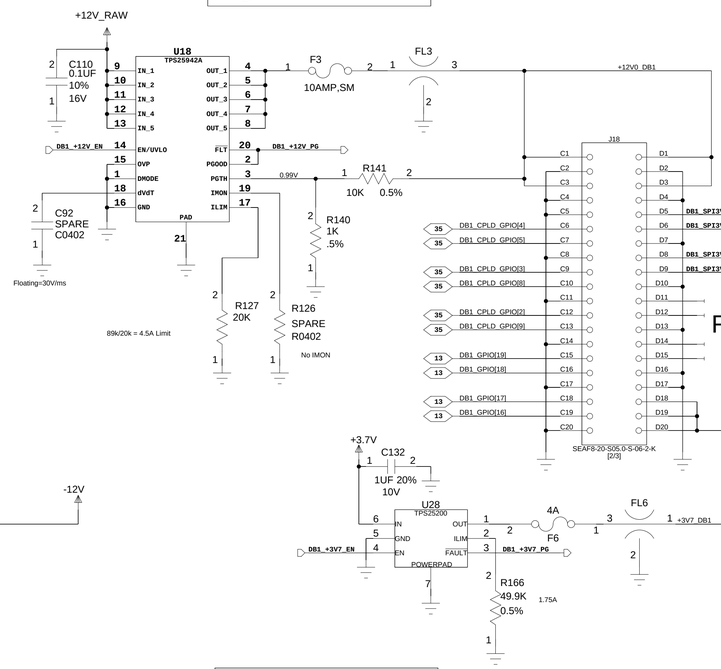


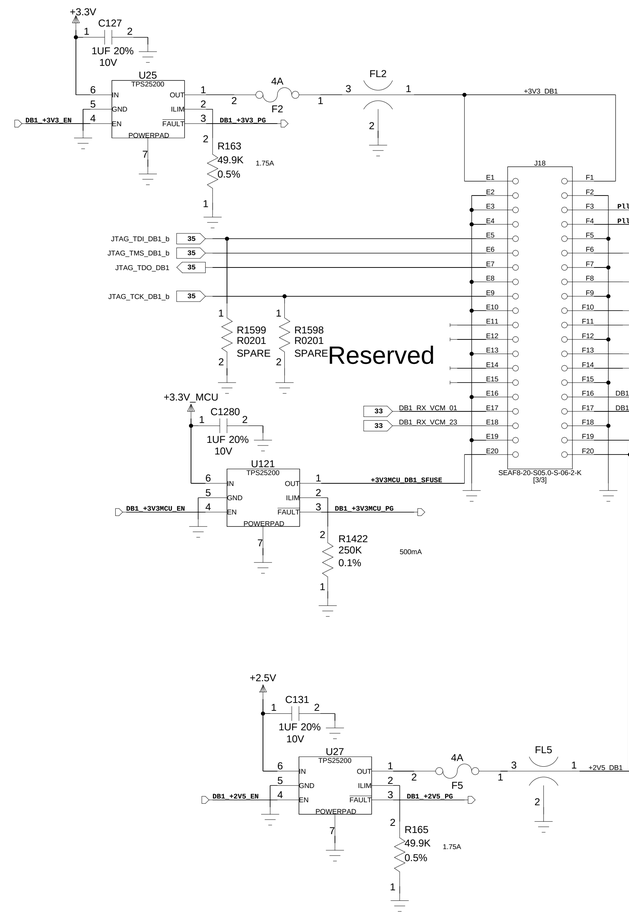




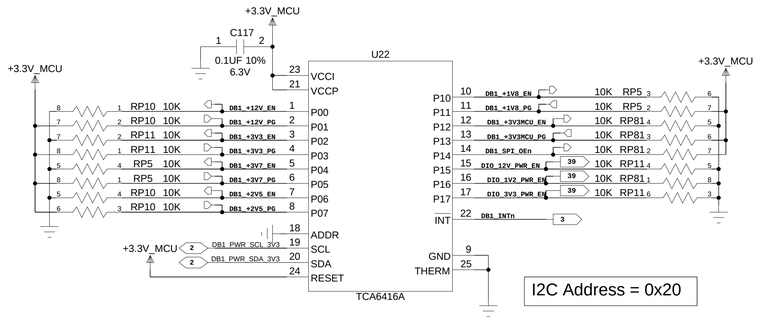
Dig Board-Board







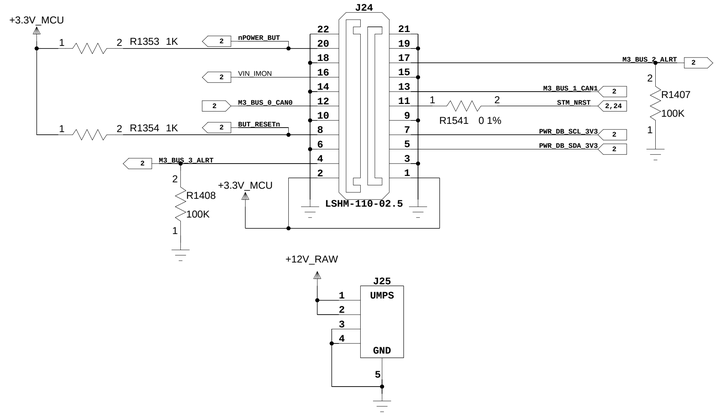
I2C GPIO Expander



POR: All Inputs
RESET Active Low!

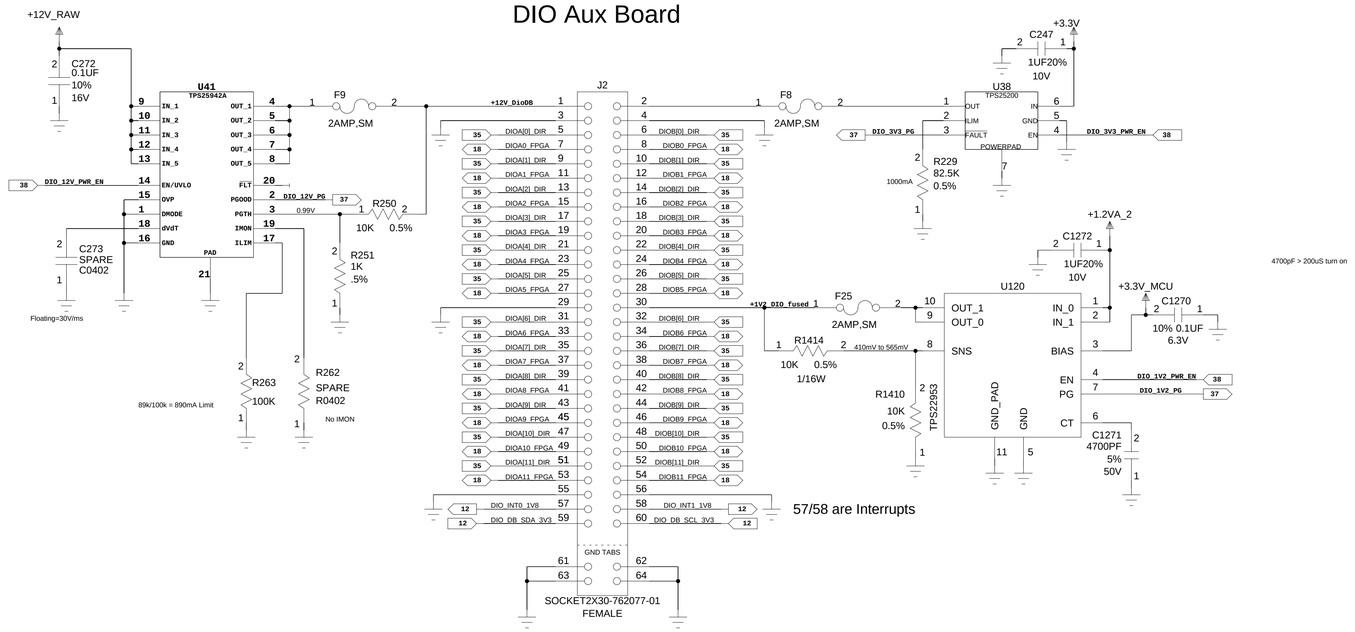
Daughtercard 1 Interface			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 37 OF 38	

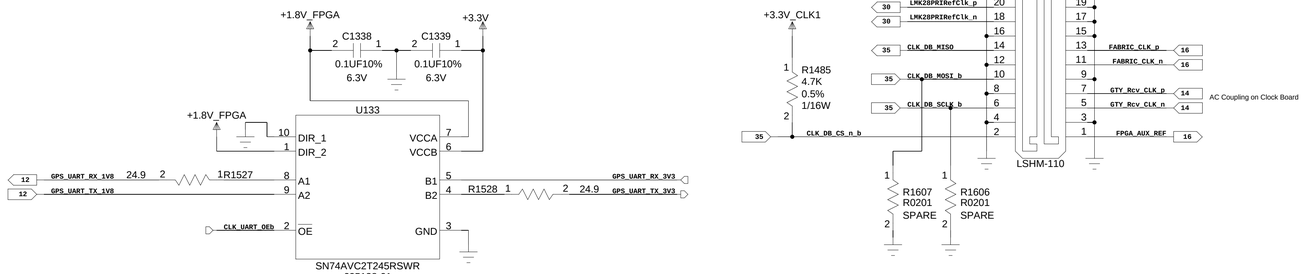
Power Aux Board



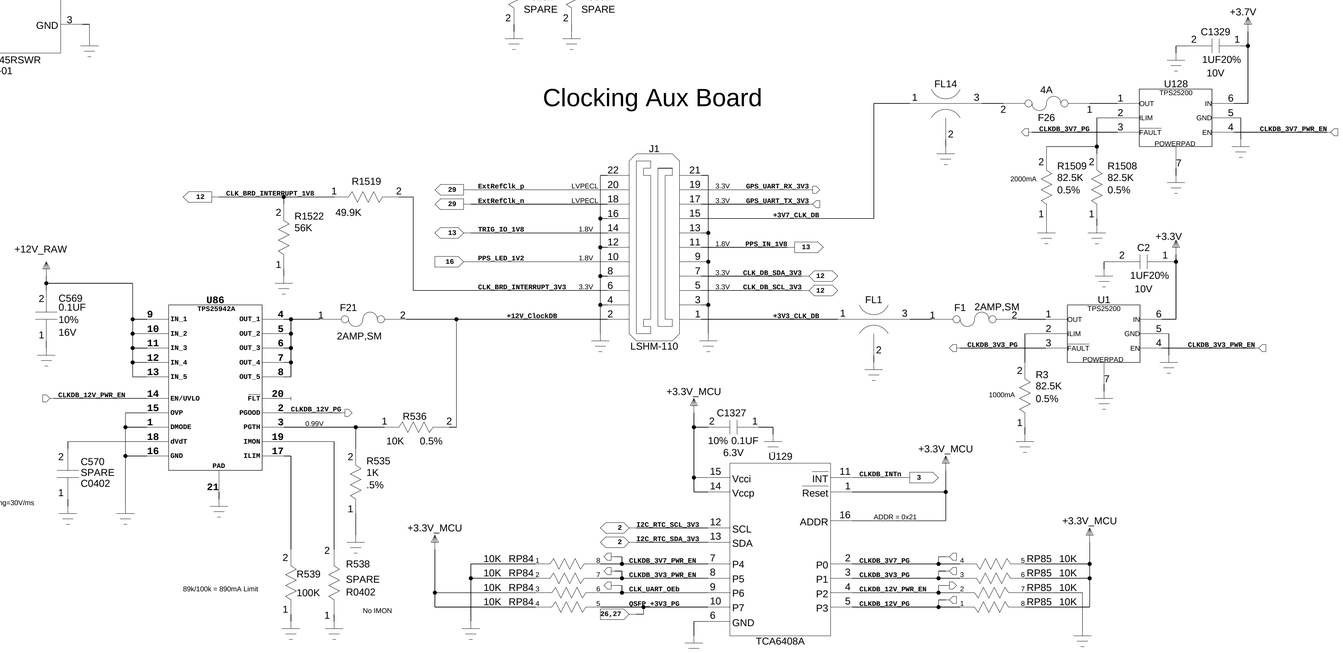
Samtec 20A Power Blade

DIO Aux Board





Clocking Aux Board



Clock/Power/DIO DB Interface			
USRP X410, BASECARD			
SIZE: C	CODE IDENT NO.: 7U296	DRAWING NO.: 146983*-01	REV: 6
SCALE: NONE		SHEET 38 OF 38	